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GENERAL MOTORS CORP GOLETA CALIF DELCO ELECTRONICS DIV  
GENERATOR SET, 100KW FREQUENCY CONVERTER.(U)  
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DAAK02-72-C-0210

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1 OF 2  
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R75-64 ✓  
JULY 1975

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FINAL TECHNICAL REPORT  
**GENERATOR SET, 100kW ✓**  
**FREQUENCY CONVERTER**

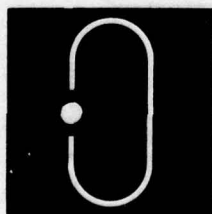
Contract CDRL Items A001 & A002

CONTRACT NO. DAAK02-72-C-0210 ✓  
(ITEM NO. 0009)  
~~XXXXXXXXXX~~

Submitted to  
U.S. ARMY MOBILITY EQUIPMENT  
RESEARCH AND DEVELOPMENT CENTER  
Fort Belvoir, Virginia

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JAN 26 1977  
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**Delco Electronics ✓**

General Motors Corporation  
- Santa Barbara Operations  
Santa Barbara, California

Goleta, Calif

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9 FINAL TECHNICAL REPORT.

6 GENERATOR SET, 100kW  
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# Delco Electronics

General Motors Corporation  
- Santa Barbara Operations  
Santa Barbara, California

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# TABLE OF CONTENTS

<u>SECTION</u>	<u>PAGE</u>
Statement of Work	1
Task 1	1
Task 2	7
Figures and Tables	
Thyristor, Diode, and Capacitor Selection Cost Study	
Task 3 Design and Test Data, Sequence A002	
Appendix A Purchase Description (Attachment 5 of Contract)	
Appendix B "A Step Forming Circuit for Sine Wave Inverters"	

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This volume of the Final Technical Report details the addition of Item 0009 considerations under Contract DAAK02-72-C-0210.

## STATEMENT OF WORK

Modification P00011 amends the basic contract to add Item 0009 as noted below:

### ITEM 0009

The Contractor shall furnish all engineering labor, tools, services, supplies, materials, equipment, and facilities necessary to perform an investigation and study of means to extend the capability of the contractor's existing Power Center Inverter System to the 100 kW level. This 100 kW Inverter System shall meet the basic performance parameters of the frequency converter covered in Paragraphs 3.5 through 3.5.3.3 of Attachment No. 5. This effort will be accomplished through the following tasks:

#### TASK 1

- a. Fabricate a breadboard of the power center inverter section to demonstrate proper operation at the 100 kW level. This approach shall use SCRs.
- b. Perform testing on the inverter breadboard circuits.
- c. Identify problem areas which will need to be analyzed to assure proper 100 kW power conditioner operation.
- d. Identify cost of components used and provide recommendations to lower the production cost of a 100 kW power conditioner.
- e. If measured performance is deficient modify the design where practical and retest.

#### TASK 2

- a. Investigate the problems of design extrapolation for the rectifier-filter end of the 100 kW inverter.
- b. Identify problem areas for capacitors, semiconductors and magnetic components.

- c. Where practical, fabricate breadboard hardware to provide a demonstration of the theoretical approach and identify hardware feasibility.

### TASK 3

Include all design and test data obtained in Final Technical Report, Sequence A002.

### TASK 1

- a. Fabricate a breadboard of the power center inverter section to demonstrate proper operation at the 100 kW level. This approach shall use SCRs.

Figures 1a and 1b are schematic diagrams of the 100 kW inverter. Figure 1a shows the thyristor and commutation network connections required for 60 Hz operation. This circuit differs from the 400 Hz circuit of Figure 1b primarily in the method used to achieve step voltage commutation. The 60 Hz circuit requires a double bus commutation circuit for the left and right voltage steps; the 400 Hz circuit employs sufficient current-voltage phase shift so that no current flows through the double bus connected thyristors. Therefore, one half the step thyristors can be disconnected from the inverter circuit. These inverter circuits were developed as a result of the work efforts of Contract Numbers DAAK02-72-C-0338 and DAAK02-72-C-0210, Items No. 0006 and 0009. All pertinent invention, design, test and synthesis work are summarized in this volume in terms of the candidate circuits of Figures 1a and 1b. The MERDC 15 kVA breadboard inverter was used as a test and design model to prove design concepts. Data generated in performing critical tests with the breadboard were used for performance extrapolations, cost analyses and problem identifications that are described in the following sections.

The circuits of Figures 1a and 1b use thyristors to perform the current switching functions. The power switch circuits are designed to produce 180/132 Vrms three phase voltages that are transformed into standard utility voltages (120/208 Vrms and 240/416 Vrms) by the output zig-zag transformer.

- b. Perform testing on the inverter breadboard circuits.

Breadboard commutation tests for a 100 kW system were conducted in a separate set of circuit experiments. Commutation of the step and power center thyristors at 600 amperes and 1000 amperes was demonstrated. The best performing commutation energy storage

circuit is illustrated in the schematic diagram of Figure 2, and commutation current paths are illustrated in Figure 3. The photographs of Figures 4 to 8 were selected to show the relationships between the load current, energy stored in the commutation network and reverse bias time for the thyristor being turned off. In addition, the influence of the bypass diode on reverse bias time and commutation current magnitude is also shown.

Figure 4 is a photograph of a step voltage change with a load current of 1,000 amperes for a step width of 540 microseconds. The load current drops to zero amperes during the commutation interval of 70 microseconds. The commutation voltage of the energy storage network Cn is shown in Figure 5 for circuits with and without bypass diode D2. The squarewave voltage has a magnitude of about 220 volts with the bypass diode and 240 volts without.

Thyristor and commutation network currents are shown in Figure 6a (with bypass diode) across the Thyristor P1 and Figure 6b (without bypass diode) for a 600 ampere load. Note that removal of the bypass diode reduces commutation circuit current by about 290 amperes. Figures 7a and 7b show reverse voltage across the thyristor during turn-off time for the conditions described in Figure 6. On a relative basis the photographs show that removal of the bypass diode increases reverse bias time; but, because of oscilloscope amplifier distortion, the photographs do not accurately indicate reverse bias time. Figures 7c through 7f illustrate the problem. The upper trace in each photograph shows bypass diode current flow. This current flows during the time that the thyristor is reverse biased. The lower trace in each photo shows thyristor reverse voltage. In Figure 7d diode current flows for about 24 microseconds, but reverse voltage is shown to appear for only 16 microseconds.

The voltage measurement problem apparently is caused by the wide voltage range that the amplifier must handle. The voltages applied across the thyristor range from +300 volts to -50 volts and we need to measure with an accuracy of one volt above and below zero reference. One solution to the problem is to clip the voltage into the amplifier when accurate measures of reverse voltage time is required. This problem requires further study, particularly if accurate measures of reapplied  $dv/dt$  at the end of the reverse bias time are to be made.

Photographs of power thyristor current into the load, energy storage network commutation current and reverse bias time for a 1,000 ampere load current are shown in Figure 8. These photographs show that an energy storage network consisting of 50  $\mu$ F, 25  $\mu$ F, and 10  $\mu$ F connected to inductors of 2  $\mu$ H, 1.2  $\mu$ H, and 1.0  $\mu$ H as shown in Figure 2, when charged to 240 volts will produce a reverse voltage bias time of more than 20 microseconds for a 1,000 ampere load. Increasing the network voltage or decreasing the load will increase the reverse voltage time.

The MERDC breadboard inverter was used as a model of the 100 kW inverter. Modeling tests at 400 Hz and 60 Hz with loads ranging from 11 kW to 28 kW were run. Performance and design data are included in Task 3 of this report.

c. Identify problem areas which will need to be analyzed to assure proper 100 kW power conditioner operation.

1) Power center thyristor commutation. The selected power center thyristor type T727 has a rated turn-off time of 20  $\mu$ seconds for the following conditions: Anode current 250A, junction temperature 125C, rate of decay  $di/dt = 50A/\mu$ sec, reapplied  $dv/dt = 20V/\mu$ sec linear to 0.8  $V_{DRM}$ . Rate of decay of the on-state current is the maximum value of the rate of decay which the thyristor may experience in establishing the turn-off time rating. Reapplied  $dv/dt$  is the minimum value of the rate of rise of forward voltage which will cause a commutation failure under specific circuit commutated turn-off conditions.

The thyristor manufacturer must be consulted to determine the rated turn-off times for the thyristors under the operating conditions that will exist in the 100 kW inverter. With this information, the design of the commutation network can be finalized.

A desirable safety factor for commutation is a reverse voltage time twice the thyristor rated turn-off time. The commutation network must carry current pulses of greater than 1,000 amperes peak with pulse widths of 60 to 80 microseconds and repetition rates of 1,200 and 2,400 Hz. Capacitor selection requires attention to heat dissipation and expected life for the required circuit operation.

Thyristor turn-off time and load current determine the required energy storage in the commutation network. The longer the thyristor turn-off time, the more costly the

commutation network. The faster the turn-off time, the higher the thyristor cost. A cost tradeoff study will help determine minimum circuit costs.

One method of reducing required commutation energy storage is use of a commutation current transformer as suggested by M. Akamatsu, et al, in USASTCFEO Report No. 2253-03857. With this method a current transformer is employed to reduce current flow in the bypass diodes with the result that energy stored in the commutation network is used more efficiently. Experiments conducted during this program at power levels up to 30 kW are described on Pages 9 and 10 of Volume III of the contract final report.

2) Magnetic components. The step autotransformer, zig-zag transformer and triplen attenuator in the experimental test circuit were designed to handle power levels up to 30 kW. Magnetic components designed for the 100 kW inverter are required for full power tests. Analysis is required to determine whether or not a conventional zig-zag transformer design can be used effectively as a step up and step down autotransformer.

3) Boost voltage commutation circuit. A boost commutation circuit designed for the 100 kW inverter is required for full power tests.

4) Waveform design. Inverter waveform design analyses in which the input and output filters are considered in the harmonic content minimization calculations will lead to further reductions in inverter cost and weight.

d. Identify cost of components used and provide recommendations to lower the production cost of a 100 kW power conditioner.

The MERDC breadboard inverter was used as a model to determine voltage and current ratings of the 100 kW circuit power components. Output connections to produce 120/208 Vrms or 240/416 Vrms three phase power for the 100 kW inverter are shown in Figures 9 and 10, respectively. The nominal input dc voltage to the inverter will be 450 Vdc with a full load dc input current of about 230A rms. The MERDC model inverter was operated at 300 Vdc input voltage, input current of 38.5 A dc with an output line current of 38A rms for a load of 11 kW, 0.8 pF. Therefore, a scale factor change of 1.5 for voltage and 6 for current is used for the following oscilloscope photographs of the Component Selection and Cost Study section. The following assumptions were in selection of inverter components.

Inverter output voltage vs load current is defined by the curve of Figure 11. Maximum ambient temperature 125F (52C); maximum semiconductor heat sink temperature rise 30C; maximum junction temperature 90°C. For thyristors, maximum  $di/dt = 50A$  per microsecond. Prices are based on quantities of 10 to 99.

Results of the thyristor and diode selection and cost study for the 100 kW inverter circuit are shown in Table I. Three thyristor types and two diode types were selected. Total cost of the thyristors and diodes is \$3,932.90. Total weight and volume of the power semiconductors including heat sinks are 149.6 lb and 4,725 in<sup>3</sup>, respectively.

Table I is the result of tests, study and analysis that led to a preliminary selection of semiconductors from data in manufacturers specifications sheets. The next step is to consult with thyristor and diode manufacturers to review Table I and obtain concurrence that the selected devices or agreed upon substitutes will perform in the 100 kW inverter. Photographs of voltage and current waveforms for every power semiconductor used in the inverter have been included in this report so that the manufacturers will have accurate descriptions of the required performance of each device. With this data, strategies for reducing component semiconductor costs can be explored.

Table II lists the results of the filter capacitor selection and cost study along with cost, weight, and volume estimates for the magnetic components used in the 100 kW inverter. Capacitor manufacturers should be consulted for concurrence that the selected components will function for the expected inverter life with the defined voltage and current stresses. The manufacturer can recommend capacitor packaging combinations that may reduce cost. Total capacitor cost as determined in this study is \$2,520. Capacitor weight and volume are 165 lb and 3,675 in<sup>3</sup>, respectively.

Table II shows that weight of the magnetic components will be about 340 lb, volume will be 2,060 in<sup>3</sup>, and cost will total approximately \$1,375.

Total cost, weight, and volume of the major power components (except circuit breakers, commutation networks, and wire) for the 100 kW inverter are listed in Table III. They are \$7,828, 655 lb and 6.05 ft<sup>3</sup>, respectively.

- e. If measured performance is deficient, modify the design where practical and retest.

Experimental high current commutation tests and breadboard model tests conducted as part of Item No's. 0006 and 0009 were sufficient at this point in the development effort to demonstrate the feasibility of fabricating 100 kW, 50, 60 or 400 Hz inverters. Problem areas requiring further analysis before additional tests can be defined are stated in Section C of Task 1.

## TASK 2

- a. Investigate the problems of design extrapolation for the rectifier-filter end of the 100 kW inverter.

The assumed diode current waveform for the 100 kW inverter rectifier is shown on Page 16 of the Component Selection and Cost Study section of this report. The diode waveform indicates a peak current for 1 P. U. loads of 360 amperes. Assumed frequency of the alternator is 1600 Hz.

For the preliminary design, a three phase, two-way bridge rectifier composed of Westinghouse R6221035FJ fast-recovery diodes has been selected.

Diode rating is 350 amperes average. Total bridge rating is 1,050 amperes. Maximum required inverter current will be approximately 625 amperes for 2.5 P.U. loads. Diode recovery time is 1.5 microseconds and  $I_{FSM}$  is 4,500 amperes.

Assumed rectifier filter capacitor current waveforms are shown on Page 17 of the Component Selection and Cost Study section of this report. Two P.U. current magnitude is assumed to be 600 A rms. For the preliminary design of the rectifier output filter a configuration made up of 24 Sprague-Type 331P metallized paper dielectric capacitors was considered. Each capacitor is 100  $\mu$ F at a rated voltage of 400 Vdc and rated current of 50A rms. The capacitors are connected 12 in parallel, in series with another set of 12 in parallel. This yields a filter and a 800 Vdc rating and capable of handling 600 A rms.

- b. Identify problem areas for capacitors, semiconductors and magnetic components.

The major problem with the rectifier output filter is high cost. This filter network represents about 25 percent of the cost of the major power components.

- c. Where practical, fabricate breadboard hardware to provide a demonstration of the theoretical approach and identify hardware feasibility.

Results of breadboard model tests and extrapolation for the rectifier end of the 100 kW inverter are given on Pages 16-17 of the Component Selection and Cost Study and Pages 38-42, 73-75, of the Task 3 sections of this report.

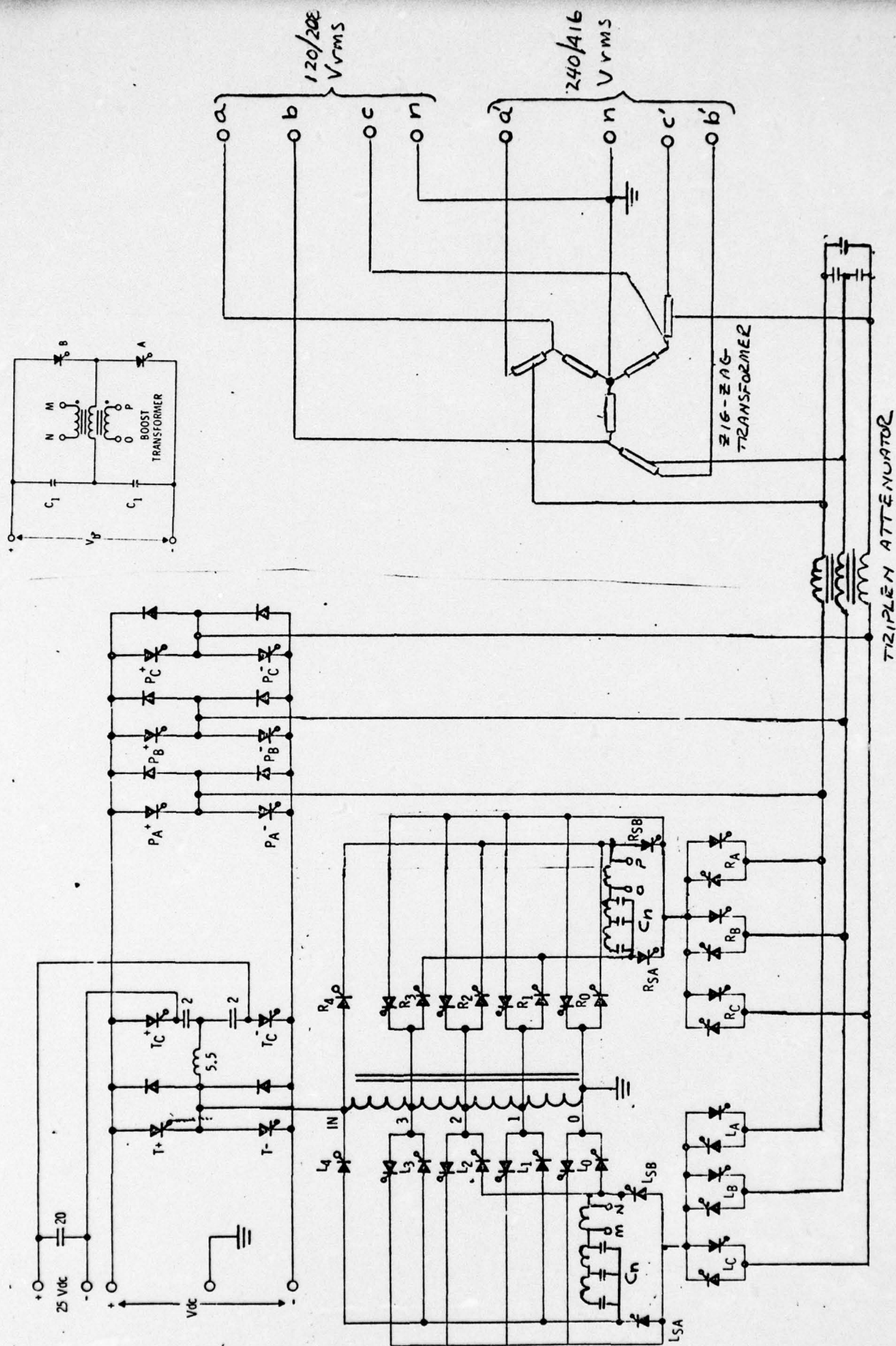


FIGURE 10. 60 HZ INVERTER CIRCUIT



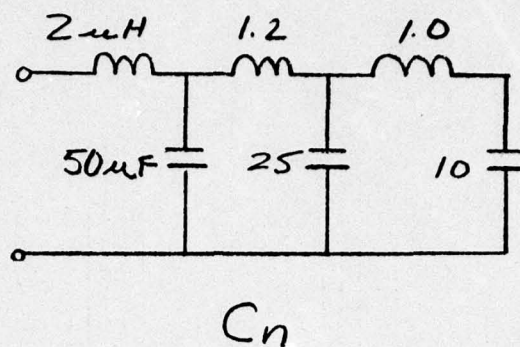


FIGURE 2. COMMUTATION ENERGY STORAGE CIRCUIT  $C_n$ .

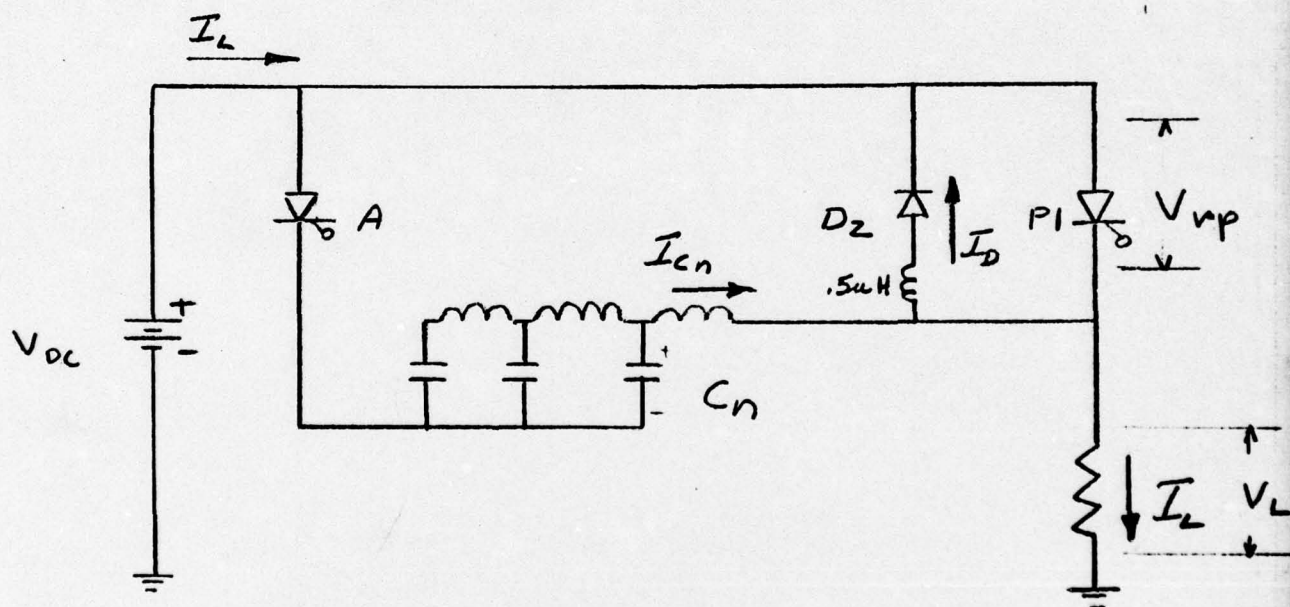


FIGURE 3. BASIC THYRISTOR COMMUTATION CIRCUIT CURRENT PATHS

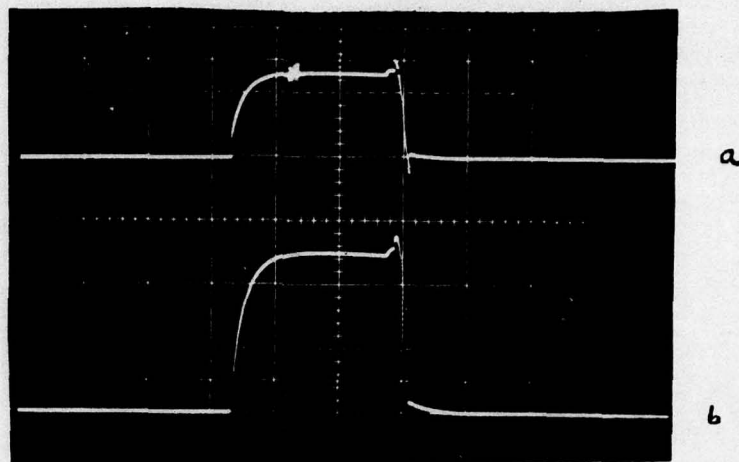
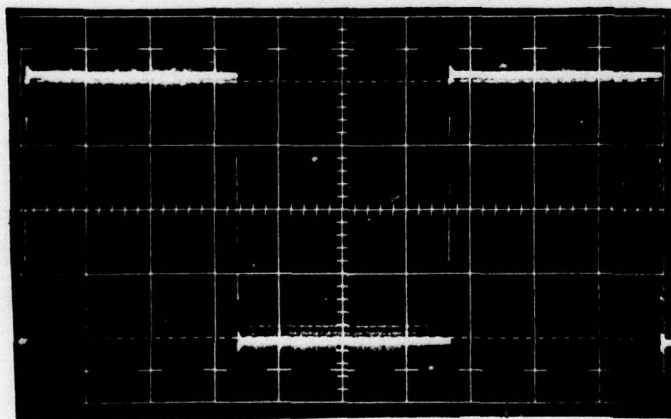
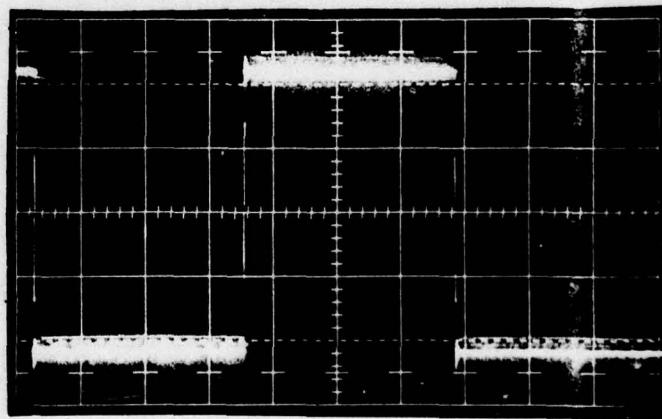
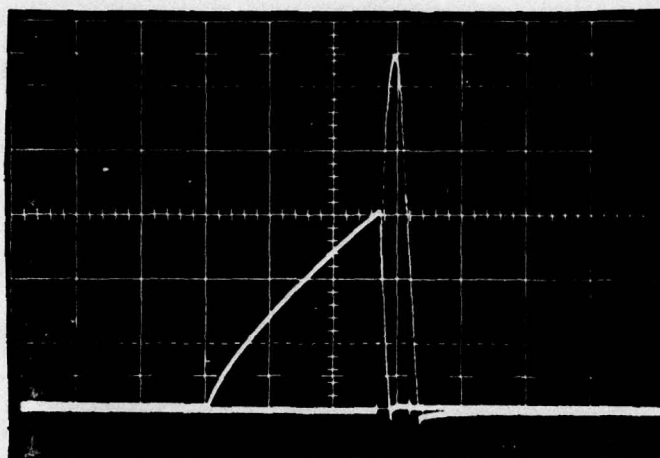


FIGURE 4

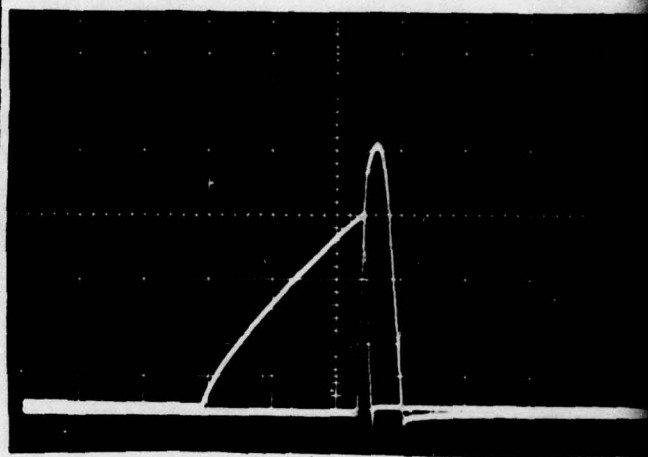
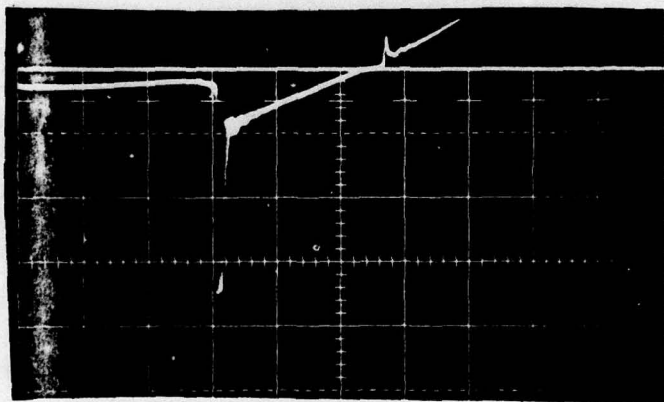
a. LOAD VOLTAGE (50V/DIV)  $V_L$ b. LOAD CURRENT (200A/DIV.  $I_L$ )TIME: 200  $\mu$ SEC/DIV.WITH BY-PASS DIODE,  $D_2$ 

WITHOUT BY-PASS DIODE

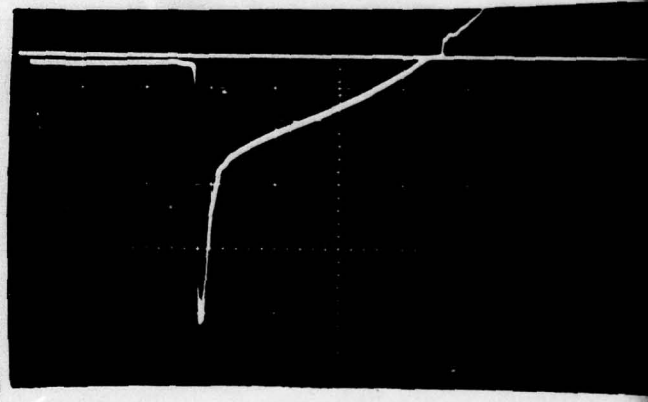
FIGURE 5. VOLTAGE ACROSS  $C_n$ . (200V/DIV. 5MS/DIV.) 1000 AMP. LOAD

WITH BY-PASS DIODE,  $D_2$ a PI CURRENT |  $C_n$  CURRENT

WITHOUT BY-PASS DIODE

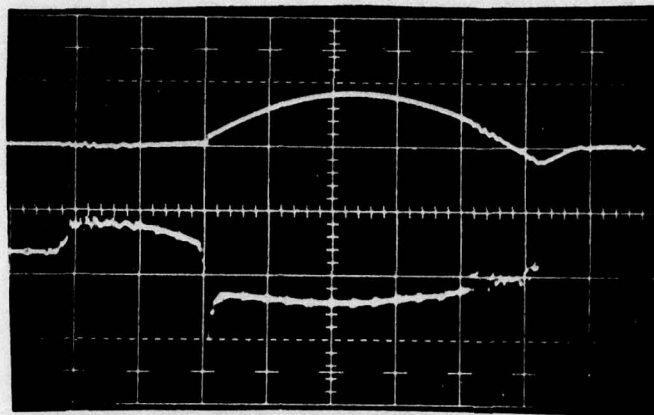
b PI CURRENT |  $C_n$  CURRENTFIGURE 6.  $P_I$  AND  $C_n$  CURRENTS. (200A/DIV. 100  $\mu$ SEC/DIV.) 600A. LOAD

a.

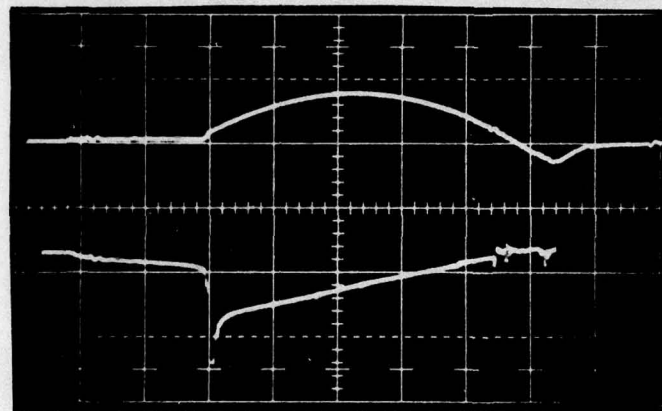


b.

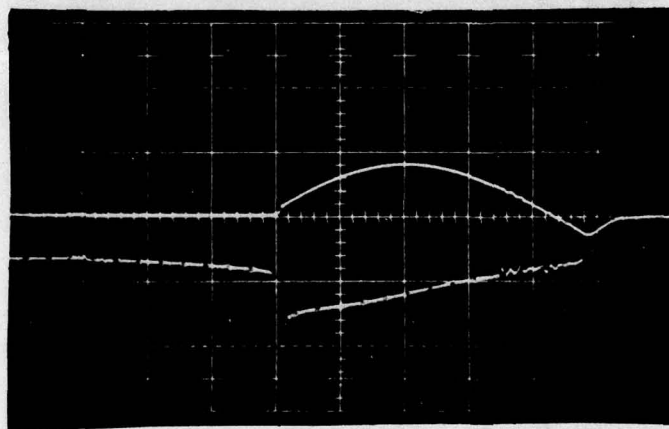
FIGURE 7. REVERSE VOLTAGE  $V_{rp}$  ACROSS THYRISTOR  $P_I$  DURING COMMUTATION. (20V/DIV. 5  $\mu$ SEC/DIV.) 600 AMP. LOAD



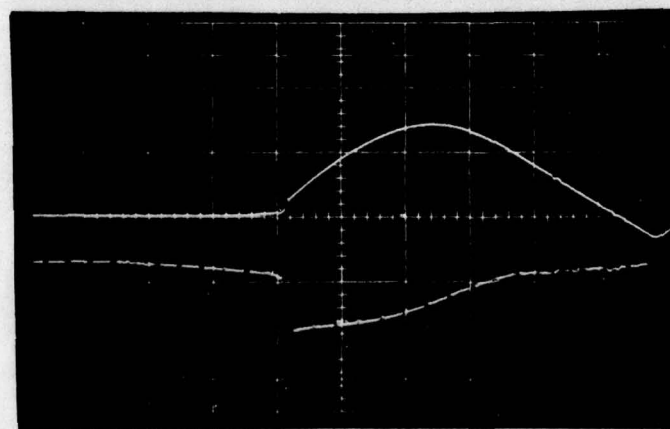
c.



d.

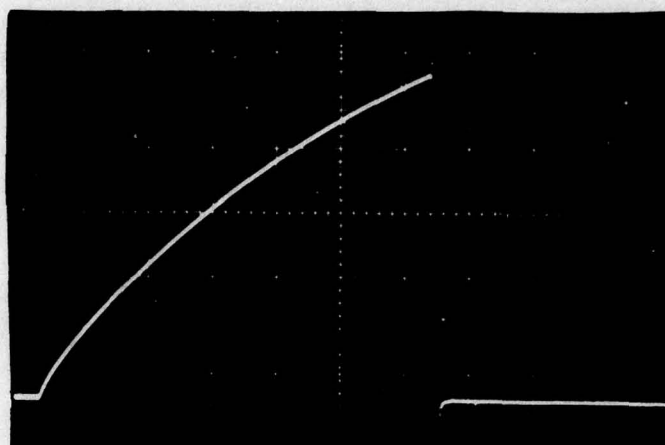


e.

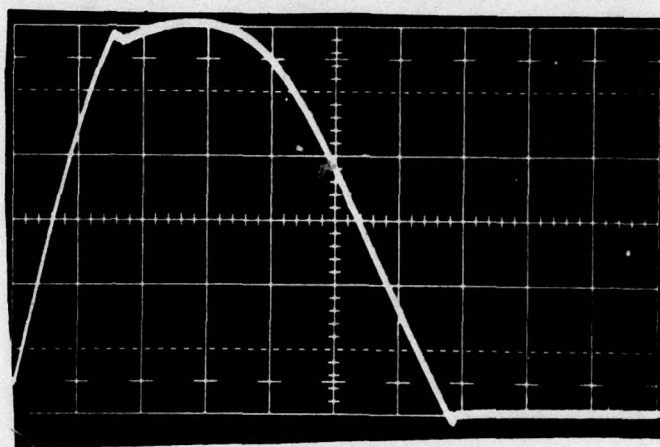


f.

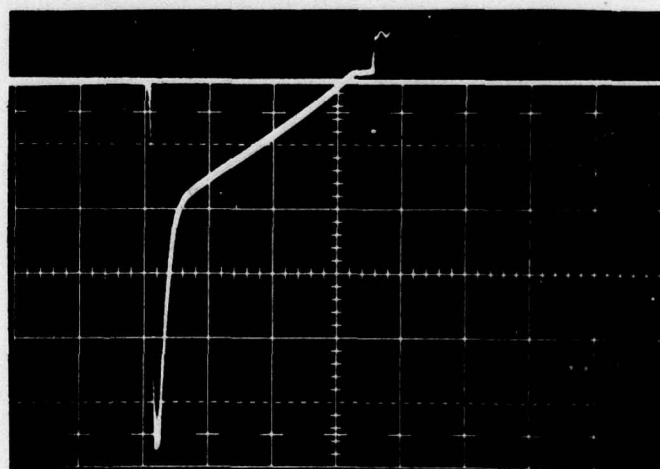
FIGURE 7. TIME SCALE 5 μSEC/DIV.



a



b



c

FIGURE 8. a) CURRENT THROUGH THYRISTOR P1. (200A/DIV. 100μSEC/DIV.)  
 b) CURRENT THROUGH  $C_n$  CIRCUIT. (200A/DIV. 10μSEC/DIV.)  
 c) REVERSE VOLTAGE  $V_{rb}$  ACROSS THYRISTOR P1 DURING  
 COMMUTATION. (50V/DIV. 5μSEC/DIV.)

CONDITIONS: 1000 AMPERE LOAD. NO BY-PASS DIODE.

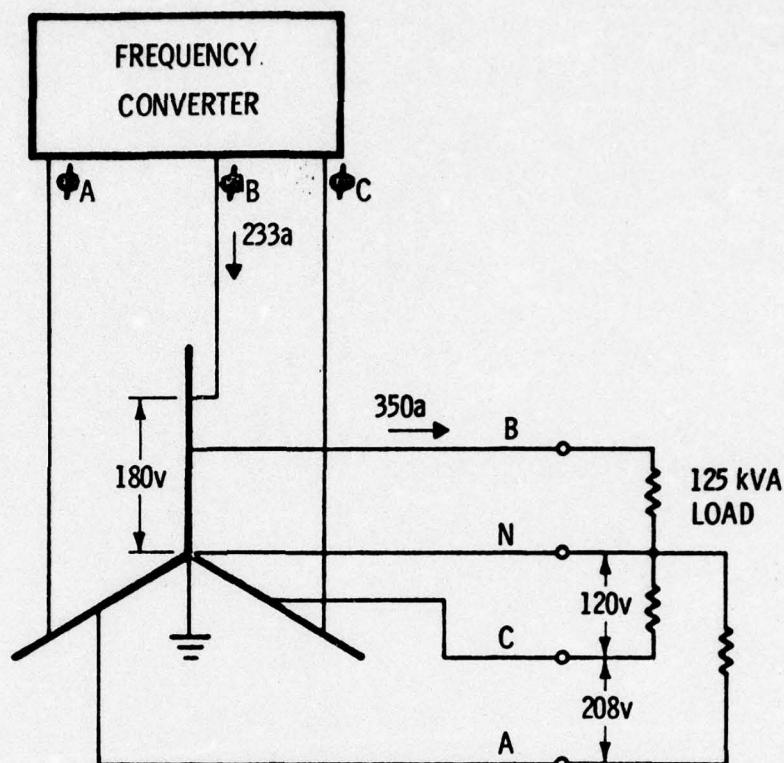


Figure 7. Frequency Converter Connection for 120/208 Vrms Three-Phase Voltages

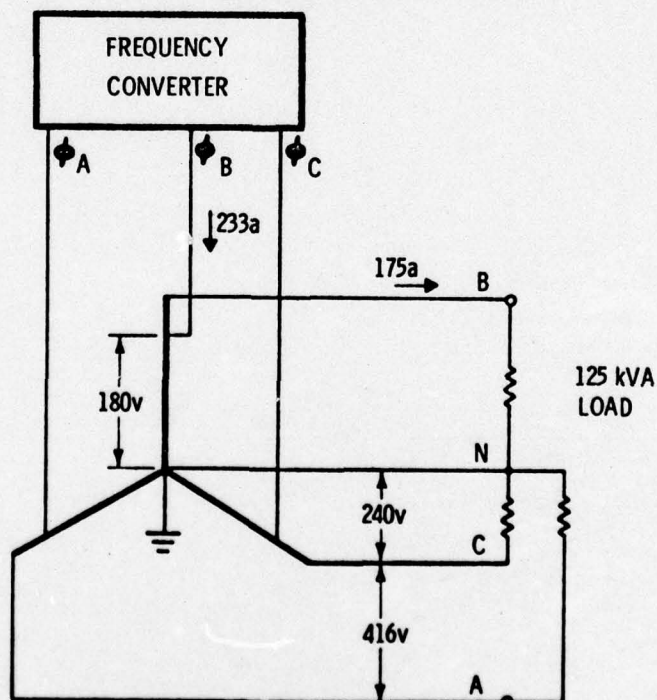


Figure 8. Frequency Converter Connection for 240/416 Vrms Three-Phase Voltages

ASSUMED INVERTER OUTPUT VOLTAGE VS LOAD  
CURRENT PROFILE

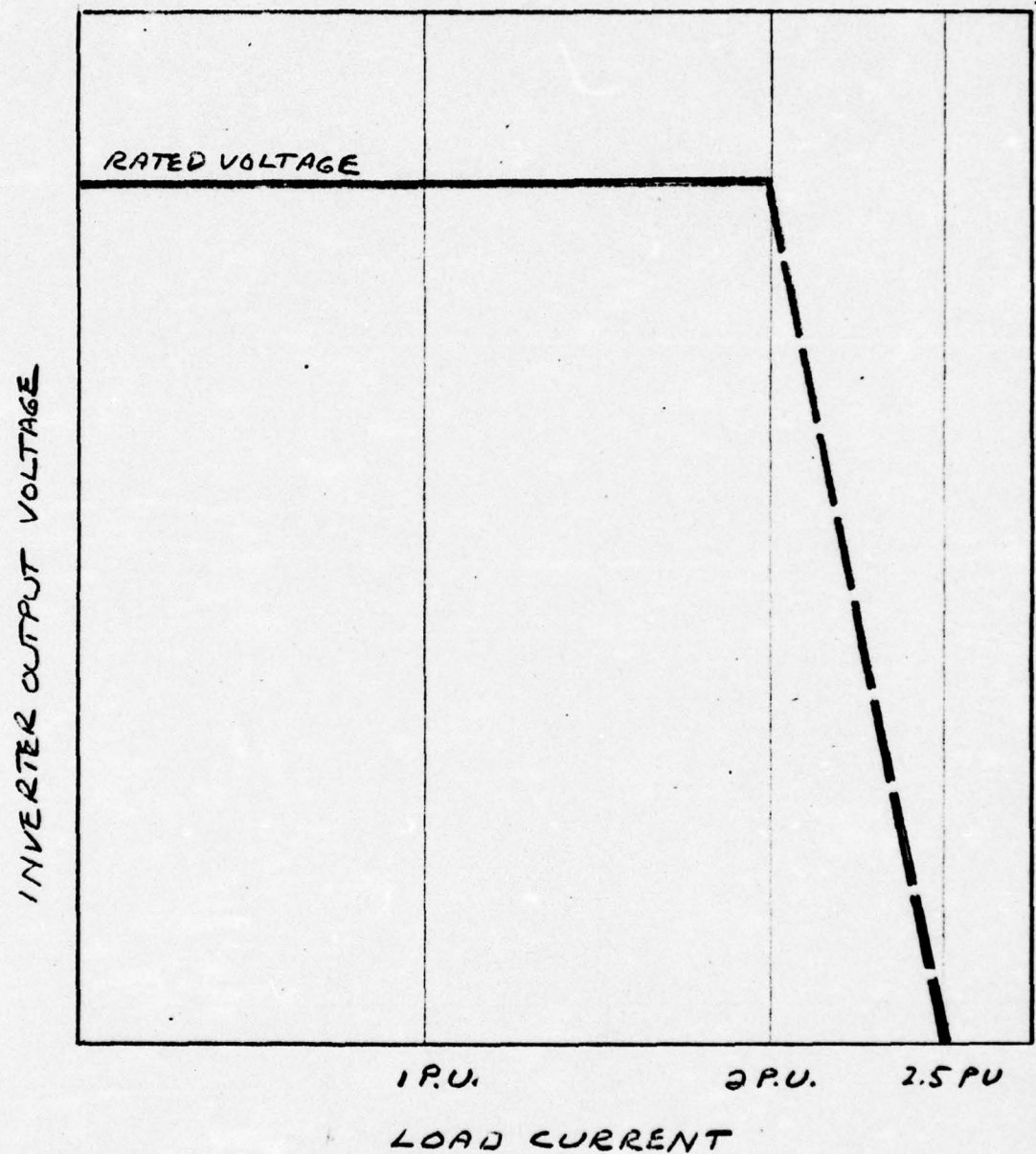


FIGURE 11

TABLE 1

SEMICONDUCTOR COMPONENT	TYPE	QUANTITY	COST PER UNIT (\$)	TOTAL COST (\$)	WEIGHT (lb)	VOLUME (in <sup>3</sup> )
POWER CENTER THYRISTOR P <sub>A</sub> <sup>+</sup> , P <sub>A</sub> <sup>-</sup> , P <sub>B</sub> <sup>+</sup> , P <sub>B</sub> <sup>-</sup> , P <sub>C</sub> <sup>+</sup> , P <sub>C</sub> <sup>-</sup>	T 727072564 DN	6	100.49	602.94	19.2	600
THYRISTOR T <sup>+</sup> , T <sup>-</sup>	T 727072564 DN	2	100.49	200.98	12.0	400
DOUBLE BUS STEP THYRISTOR L <sub>0</sub> , L <sub>1</sub> , L <sub>2</sub> , L <sub>3</sub> R <sub>0</sub> , R <sub>1</sub> , R <sub>2</sub> , R <sub>3</sub>	T 627072034 DN	8	52.15	417.20	18.6	560
FREE BUS STEP THYRISTOR L <sub>0</sub> , L <sub>1</sub> , L <sub>2</sub> L <sub>3</sub> , R <sub>0</sub> , R <sub>1</sub> , R <sub>2</sub> , R <sub>3</sub>	T 727052554 DN	8	68.69	549.52	18.6	560
PHASE SELECTOR THYRISTOR R <sub>A</sub> , R <sub>B</sub> , R <sub>C</sub> , L <sub>A</sub> , L <sub>B</sub> , L <sub>C</sub>	T 727072534 DN	12	83.74	1004.88	26.4	840
THYRISTOR L <sub>4</sub> , R <sub>4</sub>	T 627082534 DN	2	61.06	122.12	6.4	200
STEP COMMUTATION THYRISTOR R <sub>SA</sub> , R <sub>SB</sub> , L <sub>SA</sub> , L <sub>SB</sub>	T 727084554 DN	4	114.48	457.92	8.8	280
BOOST VOLTAGE THYRISTOR A, B	T 72706354 DN	2	77.59	155.18	12.0	400
THYRISTOR T <sub>C</sub> <sup>+</sup> , T <sub>C</sub> <sup>-</sup>	T 507107064	2	59.78	119.56	2.0	60
GY-PASS DIODE	R 5020810 FJ	8	18.70	149.60	1.6	80
RECTIFIER DIODE	R 6221035 FJ	6	25.50	153.00	29.0	745
* TOTAL PER CATEGORY, INCLUDES HEAT SINK WT. & VOLUME.					149.6 lb	4725 in <sup>3</sup>

TABLE II

COMPONENT	TYPE	QUANTITY	COST PER UNIT (\$)	TOTAL COST (\$)	WEIGHT (lb)	VOLUME* (in <sup>3</sup> )
INPUT FILTER CAPACITOR	331P23	24	80	1920	76	1700
OUTPUT FILTER CAPACITOR	330P35	12	50	600	89	1975
STEP AUTO-TRANSFORMER		1	200 <sup>±</sup>	200	40	360
216-2A6 TRANSFORMER		1	1000 <sup>Δ</sup>	1000	250	1250
TRIPLER ATTENUATOR		1	175 <sup>□</sup>	175	50	450
				13895	505 lb.	5735 in <sup>3</sup>

# @ \$5/16

Δ @ \$4/16.

□ @ \$3.50/16

\* 9 in<sup>3</sup>/16

TABLE III

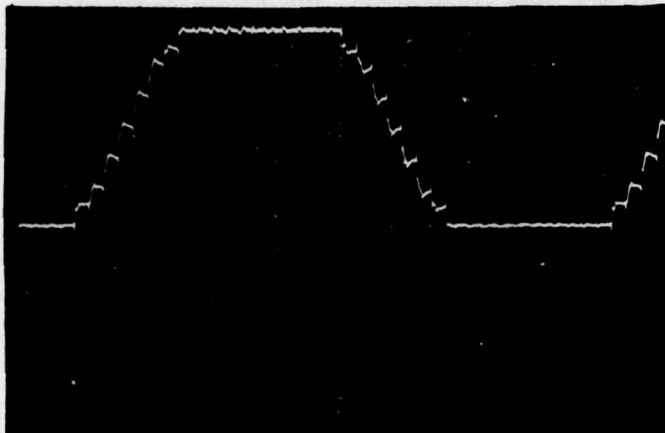
COMPONENT	COST (\$)	WEIGHT (lb)	VOLUME (IN <sup>3</sup> )
POWER SEMICONDUCTORS	3933	150 <sup>#</sup>	4725 <sup>#</sup>
INPUT & OUTPUT FILTER CAPACITORS	2520	165	3675
TRANSFORMERS	1375	340	2060
TOTAL	\$7828	655 lb	10,460 IN <sup>3</sup> 6.05 FT <sup>3</sup>

COST, WEIGHT AND VOLUME OF MAJOR POWER COMPONENTS (EXCEPT CIRCUIT BREAKERS, COMMUNICATION NETWORKS AND WIRE)

# INCLUDES HEAT SINK WEIGHT & VOLUME

**Thyristor, Diode and Capacitor Selection and  
Cost Study for the 100 kW Inverter**

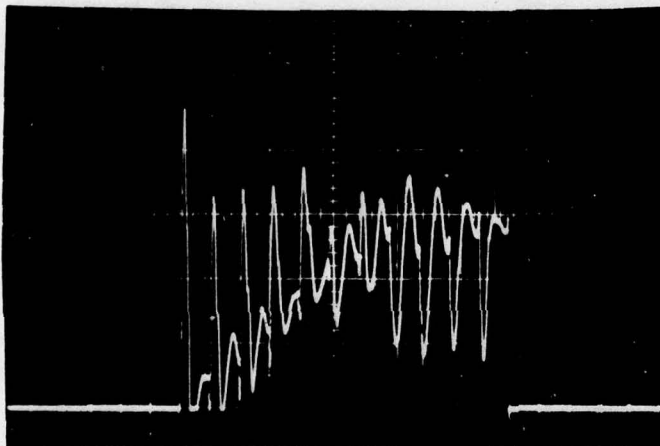
POWER CENTER THYRISTORS



THYRISTOR VOLTAGE 150V/DIV. 2MS/DIV.

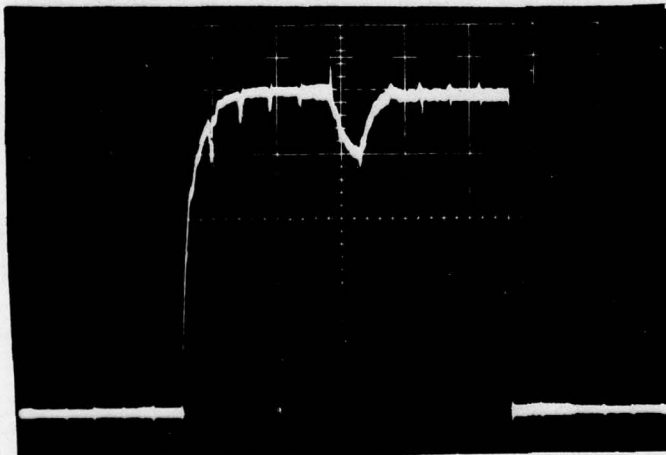
MAXIMUM THYRISTOR  
VOLTAGE = 450V.

SELECT THYRISTOR  
RATED AT 700VOLTS



1 P.U. CURRENT 120A/DIV. 1MS/DIV.

DESIRED TURN-OFF  
TIME = 15 $\mu$ SEC.



2.5 P.U. CURRENT 120A/DIV. 1MS/DIV.

MAXIMUM THYRISTOR  
CURRENT 600 A.

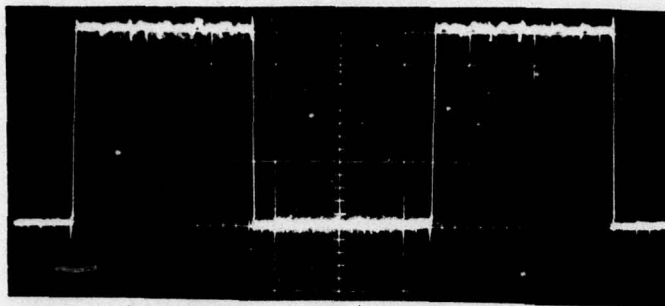
DUTY CYCLE = 0.3

250A AVG. THYRISTOR  
WILL HANDLE  
PEAK CURRENT = 680 A.  
WITH CASE TEMPERATURE  
OF 90C. AT 400 HZ.

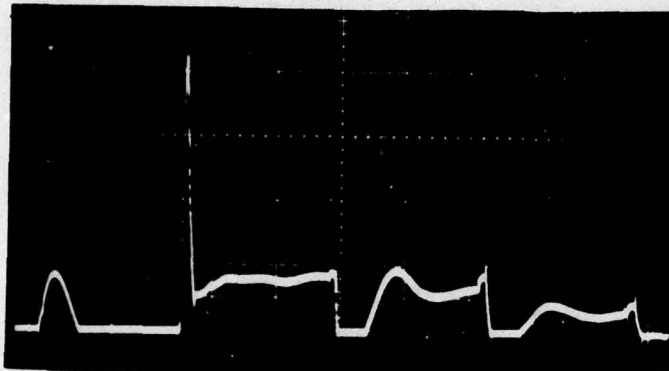
SELECT WESTINGHOUSE THYRISTOR T727072574 DN  
(700V, 250A, AVG. 15 $\mu$ SEC) THYRISTOR.

T727072564 AVAILABLE IN CATALOG. 20 $\mu$ SEC. TURN-OFF  
TIME. PRICE \$100.49.

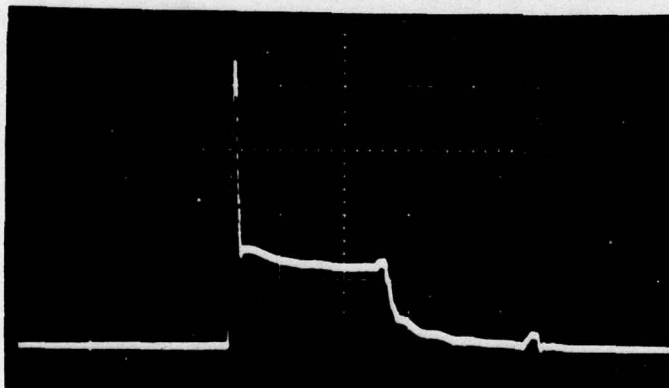
T<sub>1</sub>, T- THYRISTORS 60HZ



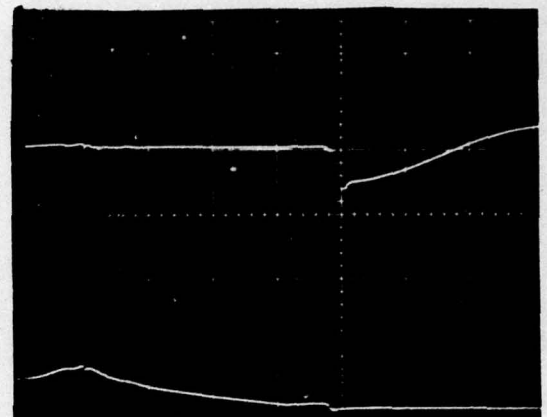
THYRISTOR VOLTAGE 150V/DIV. 1ms/DIV.



1 A.U. CURRENT 300A/DIV. 200μSEC/DIV.



2.5 A.U. CURRENT 300A/DIV. 200μSEC/DIV.



UPPER: REVERSE TURN-OFF VOLTAGE 20V/DIV.

LOWER: ANODE CURRENT 50A/DIV. 5μSEC/DIV.

MAXIMUM THYRISTOR VOLTAGE = 450V.

SELECT THYRISTOR RATED AT 700V.

DESIRED TURN-OFF TIME = 15μSEC.

FREQUENCY = 1200HZ

DUTY CYCLE = 0.25

PEAK CURRENT = 1500 AMPS.

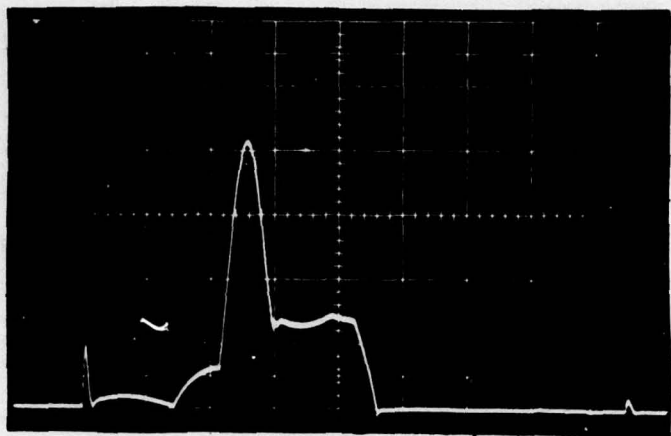
AVG. CURRENT = 50A. FOR SHORT C.T. CASE.

SELECT WESTINGHOUSE T607072574 DN (700V, 250A.AVG. 15μSEC)

THYRISTOR. WILL HANDLE 1265A. PEAK FOR 0.1 DUTY CYCLE AT 90°C OR 1800A. PEAK AT 65°C)

T607072564 (20μSEC) AVAILABLE IN CATALOG. #67.42

T<sub>1</sub>, T-THYRISTORS 400 Hz



1 P.U. LOAD

$$\text{DUTY CYCLE} = \frac{250 \mu\text{SEC}}{833 \mu\text{SEC}} \\ = 0.3$$

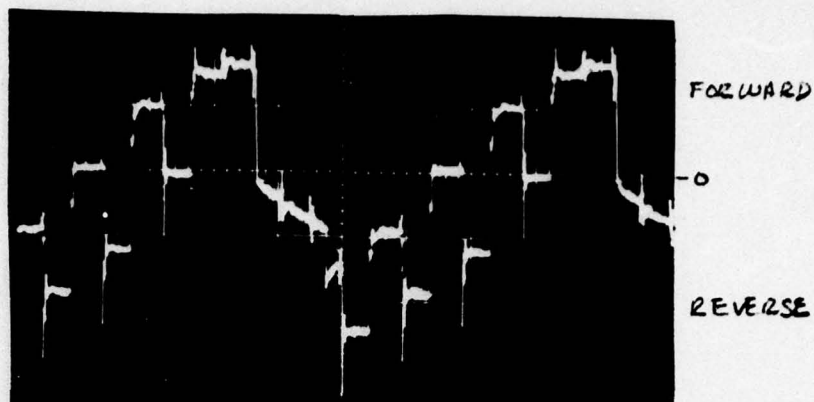
THYRISTOR CURRENT 150A/DIV. 50μSEC/DIV.

PEAK COMMUTATION CURRENT = 650A.  
MAXIMUM LOAD CURRENT AT 2 P.U. = 460A.  
FREQUENCY = 1200 Hz. DESIRED TURN-OFF  
TIME = 15 μSEC.

SELECT (W) T727072574DN

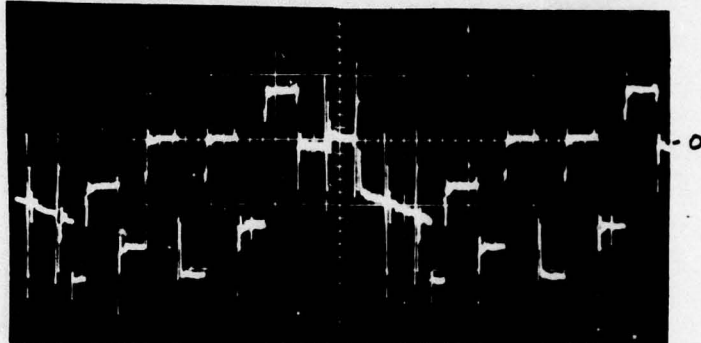
T727072564DN (20μSEC) LISTED IN CATALOG #100.49

DOUBLE BUS STEP THYRISTORS

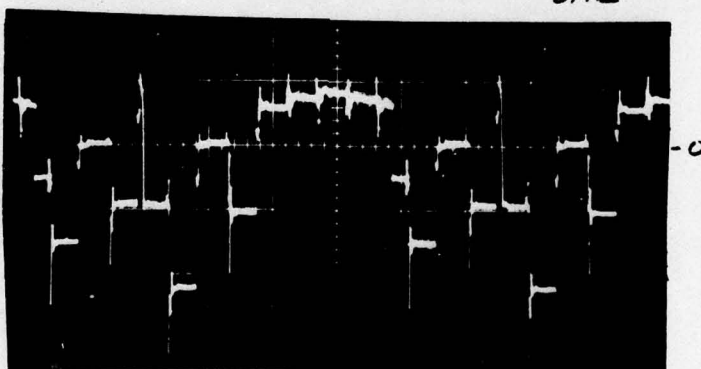


THYRISTOR VOLTAGE 60HZ

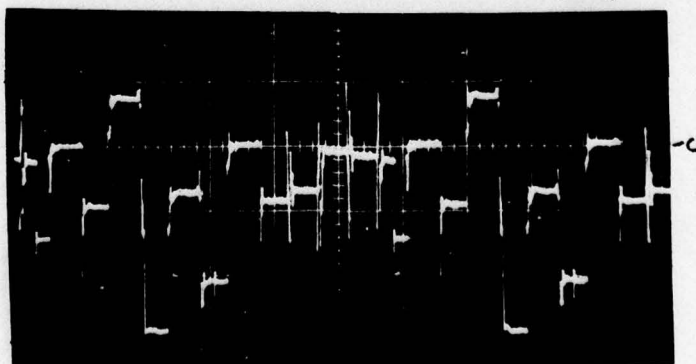
ZERO



ONE



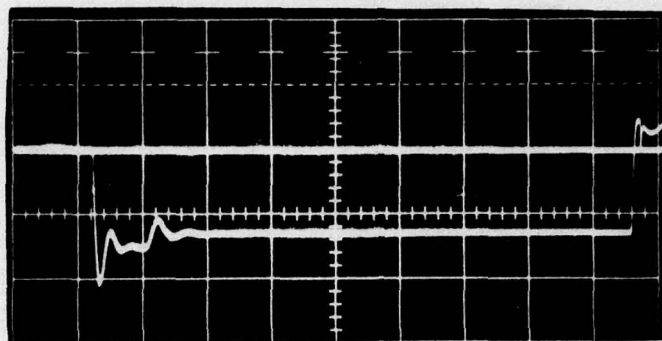
TWO



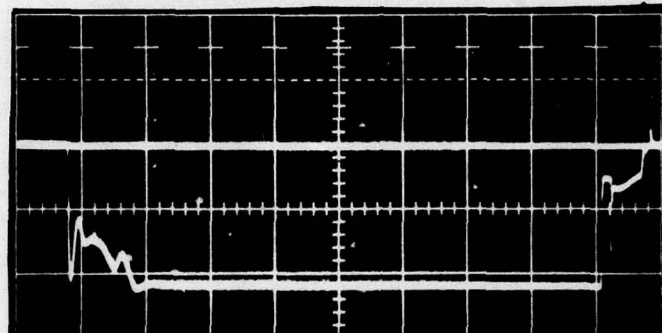
150V/DIV. 1MS/DIV.

THREE

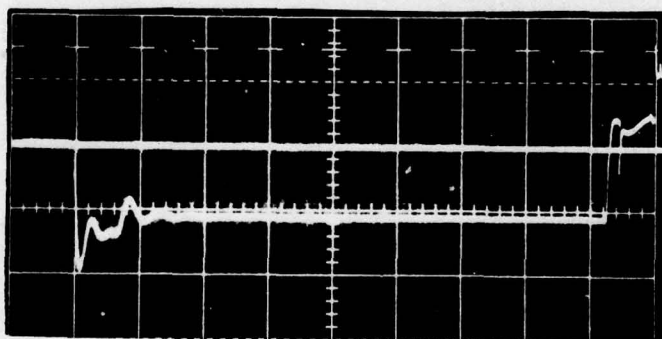
MAXIMUM THYRISTOR REV. VOLTAGE = 510V. SELECT THYRISTOR  
RATED AT 700V.



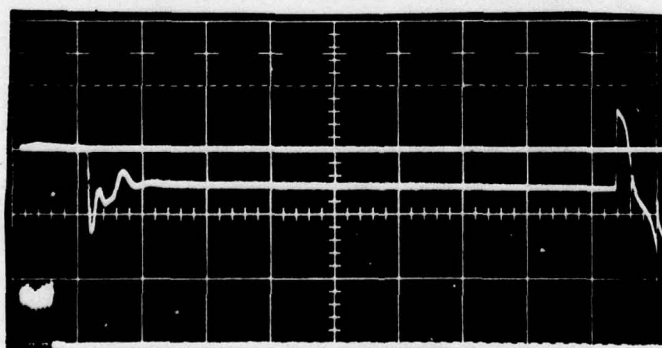
ZERO



ONE



TWO



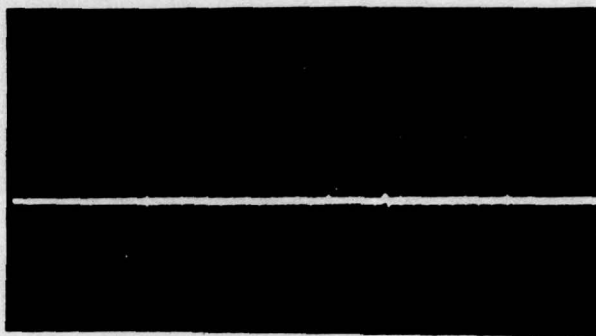
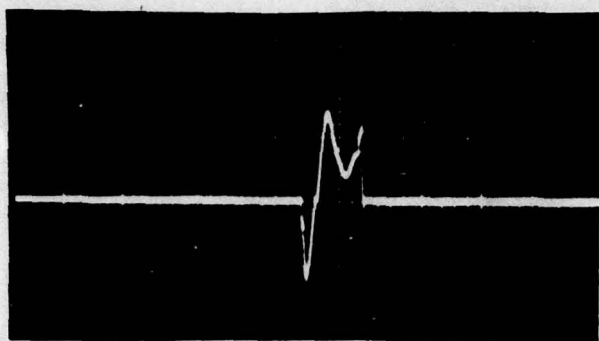
THREE

50  $\mu$  SEC/DIV.

REVERSE TURN-OFF  
VOLTAGES FOR  
STEP THYRISTORS  
DOUBLE BUS 60Hz

ALL STEP THYRISTORS  
ARE REVERSE  
BIASED AT LEAST  
400  $\mu$  SEC.

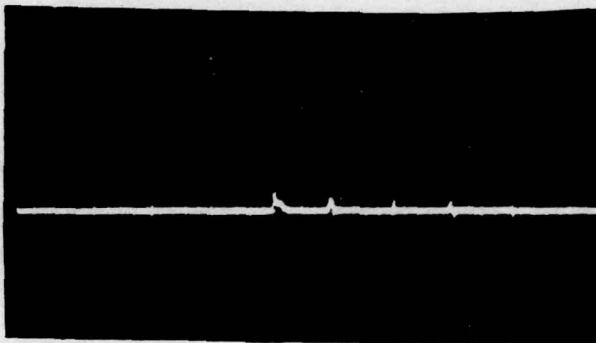
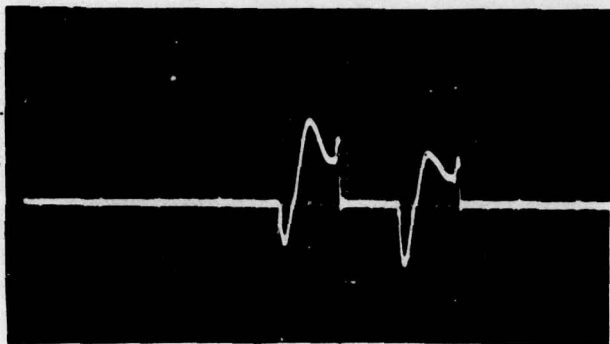
SELECT 50  $\mu$  SEC.  
THYRISTORS



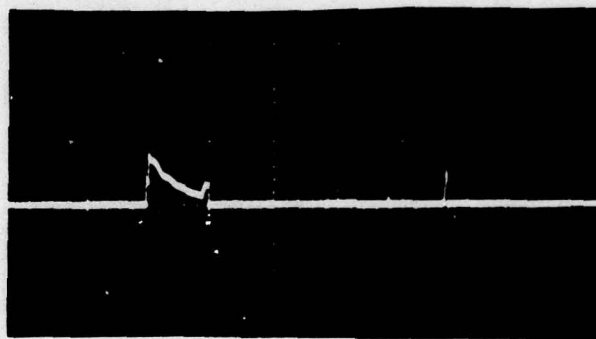
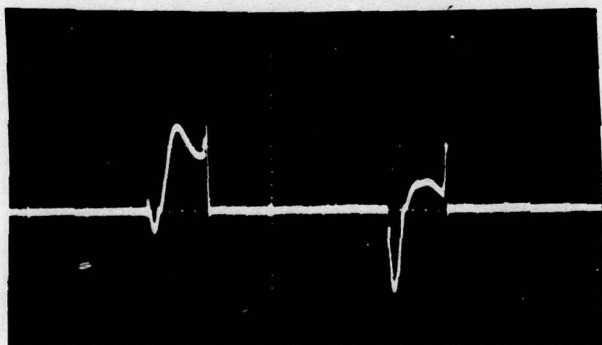
FREE BUS  
CURRENT

DOUBLE BUS  
CURRENT

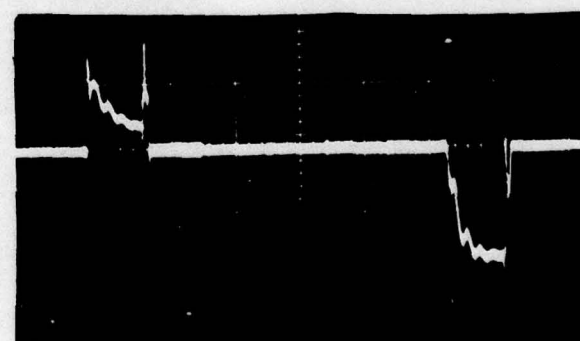
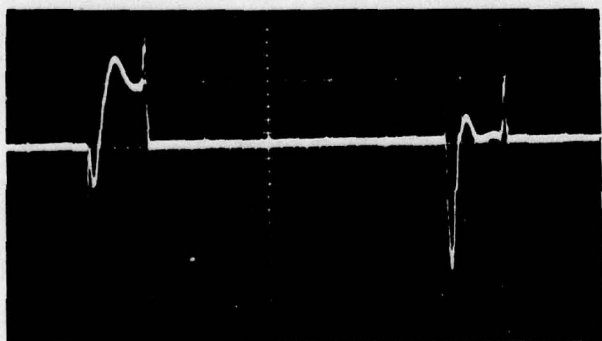
ZERO



ONE



TWO



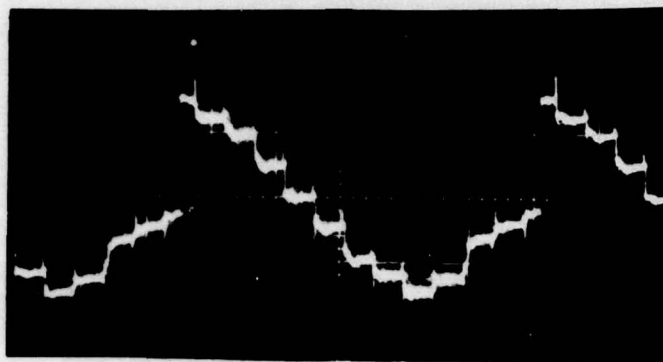
1 P.U.

THREE

2.5 P.U.

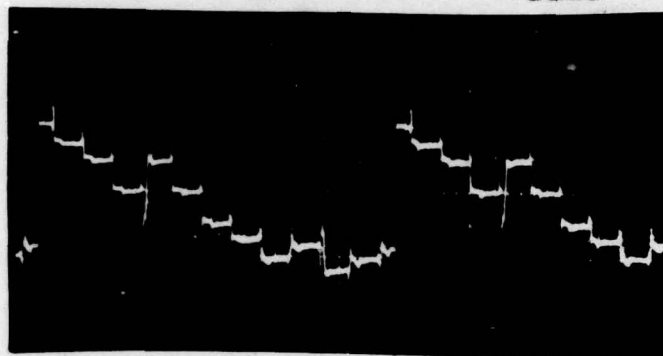
60HZ STEP THYRISTOR CURRENTS 300A/DIV. 500μSEC/DIV.  
 MAXIMUM CURRENT = 1200 AMPS AT 2 P.U. DUTY CYCLE FOR  
 THIS CASE < 0.1. FREQUENCY = 180 HZ. SELECT (W) T627072034DN  
 (700V, 200A. AVG. 5μSEC). \$52.15

# FREE BUS STEP THYRISTORS

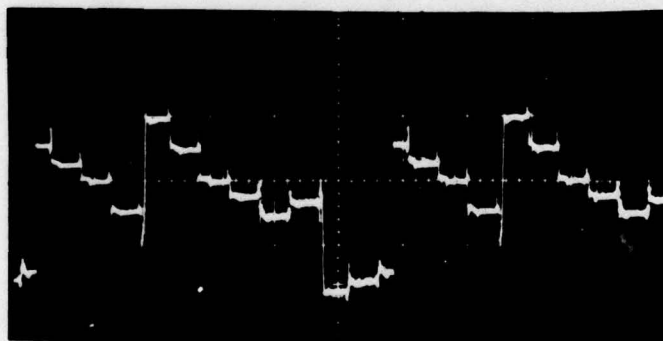


THYRISTOR VOLTAGE 60HZ

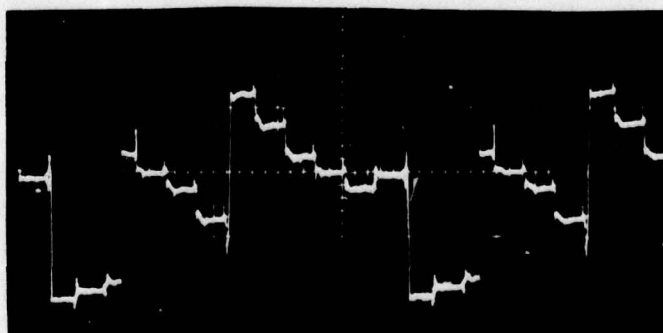
ZERO



ONE



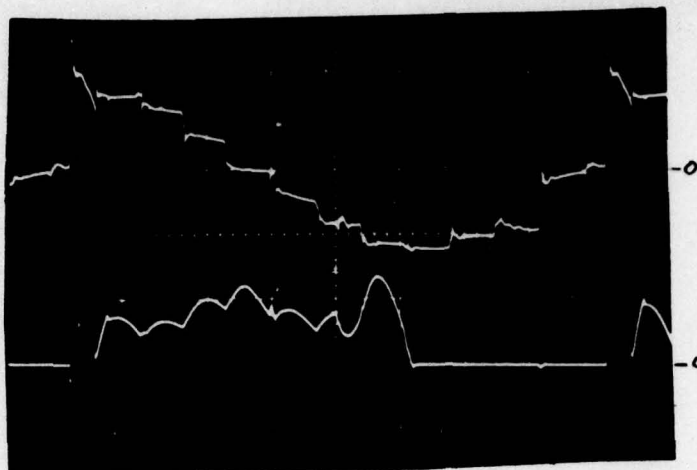
TWO



150V/DIV. 1MS/DIV.

THREE

MAXIMUM THYRISTOR REV. VOLTAGE = 300V. SELECT  
THYRISTOR RATED AT 500V.



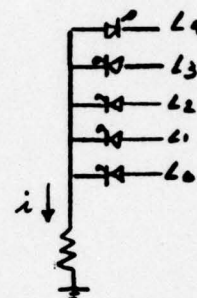
LEFT SIDE STEP VOLTAGE  
150V/DIV. 100μSEC/DIV.  
400Hz

STEP CURRENTS  
NO LOAD  
600A/DIV. 100μSEC/DIV

PC 3 2 1 0 1 2 3



1 P.U. LOAD  
600A/DIV.



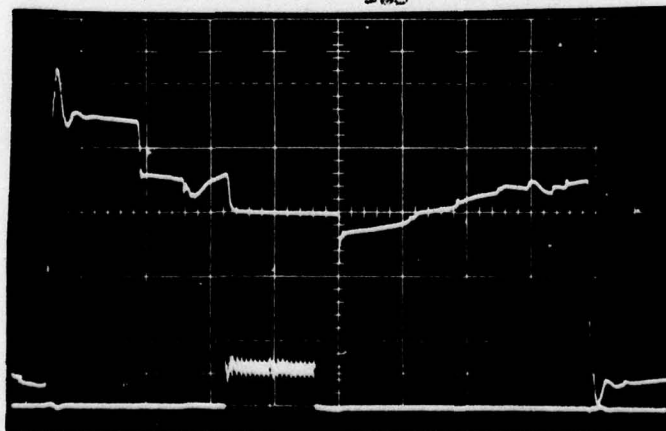
MAXIMUM CURRENT WITH 2 P.U. LOAD = 1440 A. FOR STEP 3.

STEP 3 CONDUCTS TWICE PER CYCLE AT 1200 Hz RATE.

FIRST CONDUCTION CURRENT = 960 A WITH 2 P.U. LOAD

SECOND CONDUCTION CURRENT = 1440 A WITH 2 P.U. LOAD

$$\text{DUTY CYCLE} = \frac{60^\circ}{360^\circ} = 0.167$$



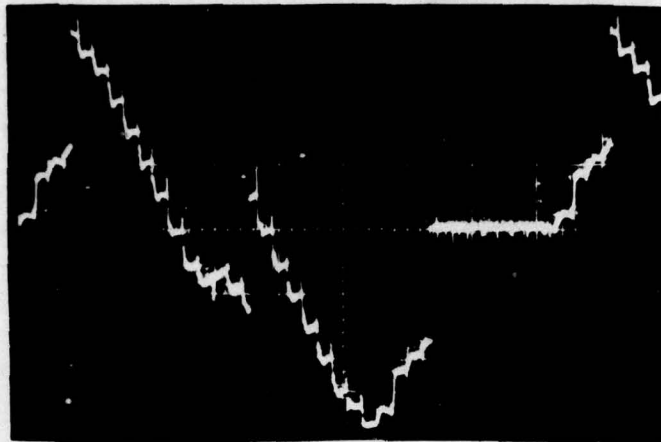
REVERSE TURN-OFF VOLTAGE FOR R3  
400Hz. 50V/DIV. 50μSEC/DIV.

DESIRED TURN-OFF TIME = 30μSEC.

SELECT (W) 727052554DN

(500V, 250A AVG. 30μSEC) 68.69

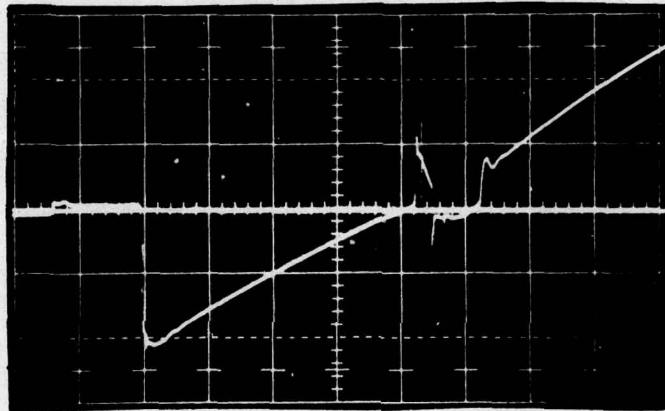
# PHASE SELECTOR THYRISTORS



THYRISTOR VOLTAGES 150V/DIV. 2MS/DIV. 60HZ

MAXIMUM VOLTAGE = 500V.

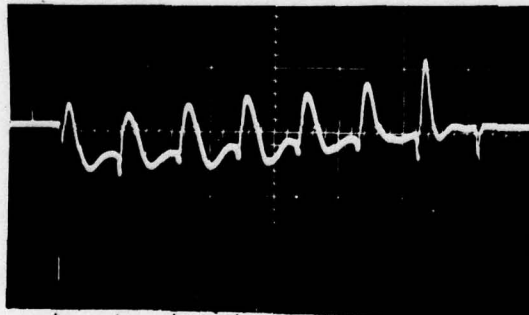
SELECT 700V THYRISTOR



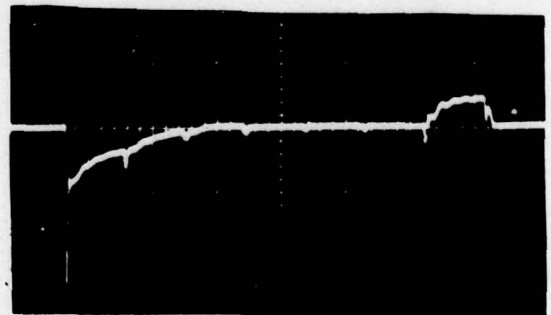
THYRISTOR REVERSE TURN-OFF VOLTAGE  
20V/DIV. 100µSEC/DIV. 60HZ

SELECT 50µSEC

TURN-OFF THYRISTOR

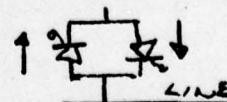


PC 3 | 2 | 1 | 0 | 1 | 2 | 3 |  
1 P.U. 600A/DIV. 0.5MS/DIV.



2.5 P.U. 600A/DIV. 0.5MS/DIV. 60HZ

THYRISTOR CURRENTS

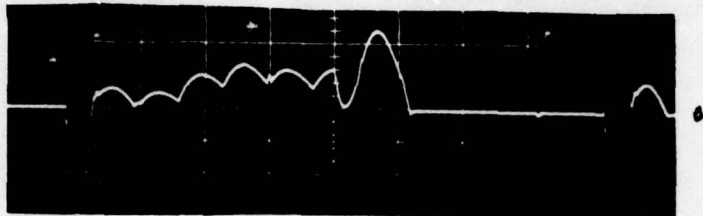


MAXIMUM 2 P.U. LOAD CURRENT = 1400 A. DUTY CYCLES ≤ 0.3

FREQUENCY = 60 HZ

SELECT @ T727072534DN

(700V, 250A.AVG, 50µSEC) #83.74



THYRISTOR CURRENT 400Hz 1 P.U.

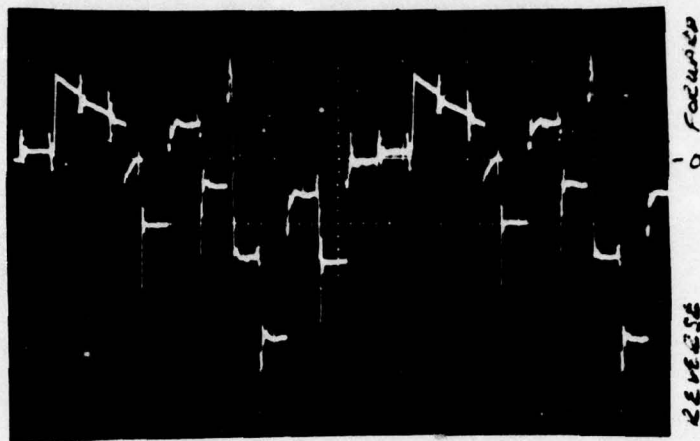
600A/DIV. 100μSEC/DIV.

MAXIMUM 2 P.U. CURRENT = 1500 AMPS

DUTY CYCLE = 0.17 FREQUENCY =

SELECT (W) T727672534 DM (700V, 250A, 50μSEC) #83.74

# POWER CENTER COMMUTATION THYRISTORS



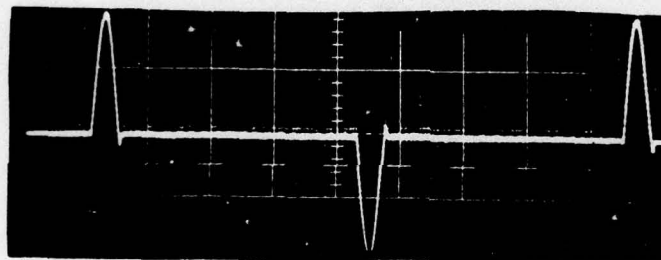
THYRISTOR VOLTAGE 150V/DIV. 1MS/DIV. 60HZ

MAXIMUM REVERSE  
VOLTAGE = 600V.

SELECT 800V THYRISTOR

REVERSE TURN-OFF  
VOLTAGE TIME 7100μSEC.

SELECT 50μSEC. THYRISTOR



THYRISTOR CURRENT 600A/DIV. 100μSEC/DIV. 400HZ

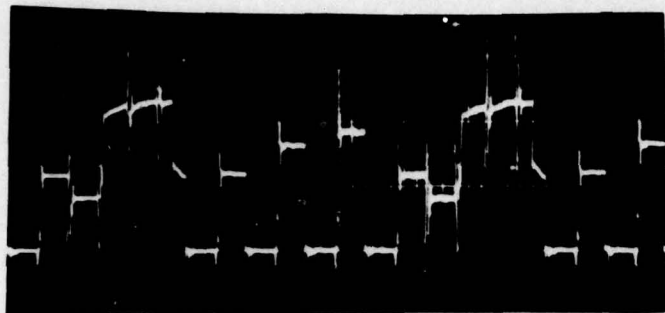
MAXIMUM CURRENT = 1200A.

FREQUENCY = 1200HZ

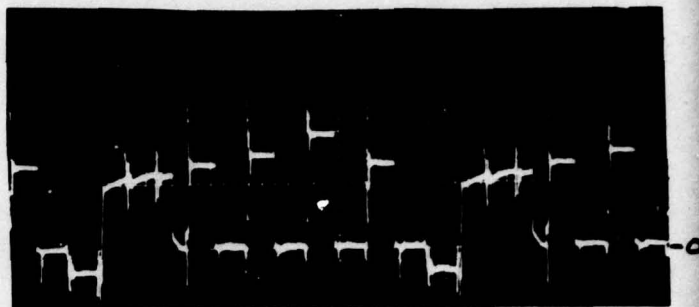
DUTY CYCLE < 0.1

SELECT T6270B2534DN (800V, 250A. AVG. 50μSEC) <sup>2</sup>61.06

# STEP COMMUTATION THYRISTORS

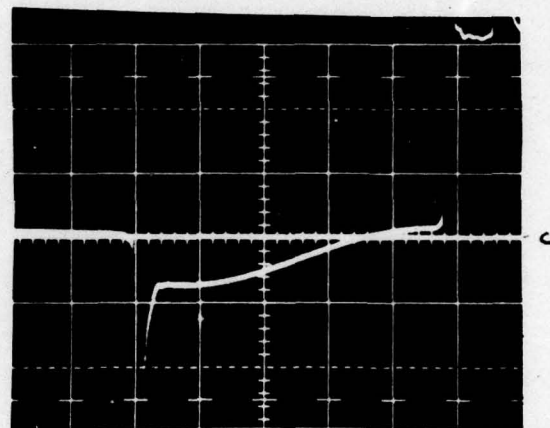
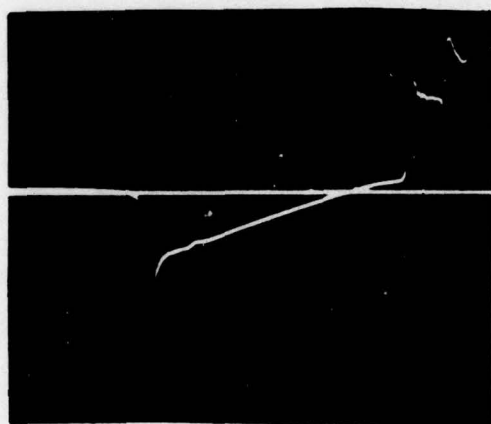


Rsa

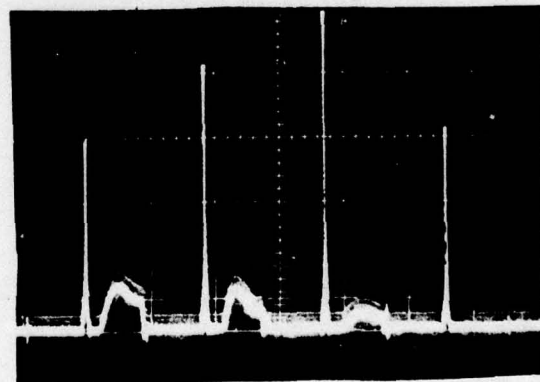
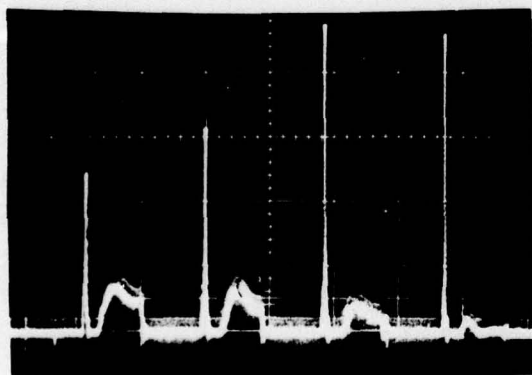


Rsb

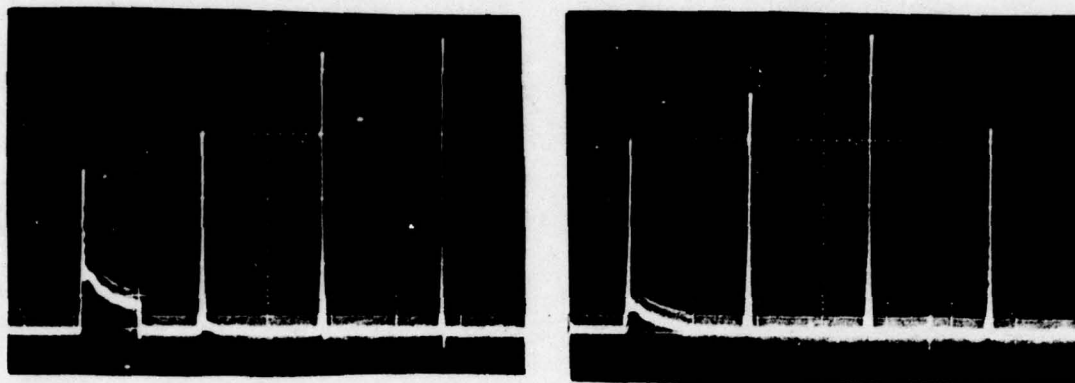
THYRISTOR VOLTAGES 150V/DIV. 1MS/DIV. 60HZ  
MAXIMUM FORWARD VOLTAGE = 510V. SELECT 800V THYRISTOR



REVERSE TURN-OFF VOLTAGE 20V/DIV. 5μSEC/DIV.  
SELECT THYRISTOR WITH 15μSEC. TURN-OFF TIME



THYRISTOR CURRENTS 1PU. 600A/DIV. 500μSEC/DIV.  
FREQUENCY = 2160HZ DUTY CYCLE = 0.32



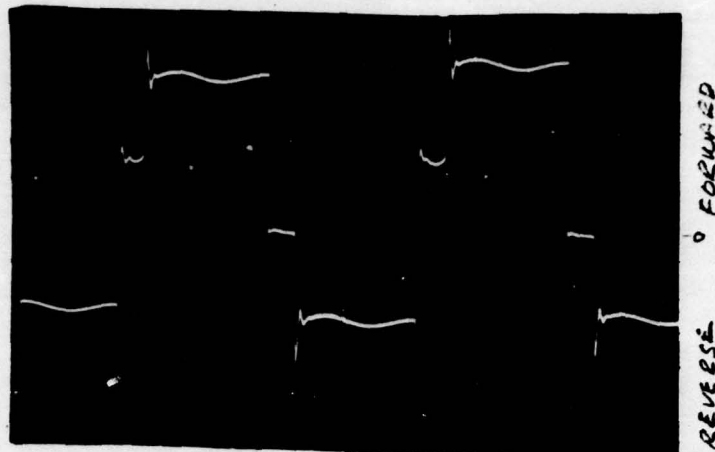
THYRISTOR CURRENTS 2.5 P.U. (SHORT CIRCUIT) 600V/DIV. 500μSEC/DIV.

MAXIMUM 2 P.U. LOAD CURRENTS 960 A. PLUS STEP COMMUTATION CURRENT PULSES 2800 A.

SELECT (W) T727084579DN (800V, 450A AVG, 15μSEC)

T727084554 (30μSEC) LISTED IN CATALOG #114.48

## BOOST VOLTAGE THYRISTORS

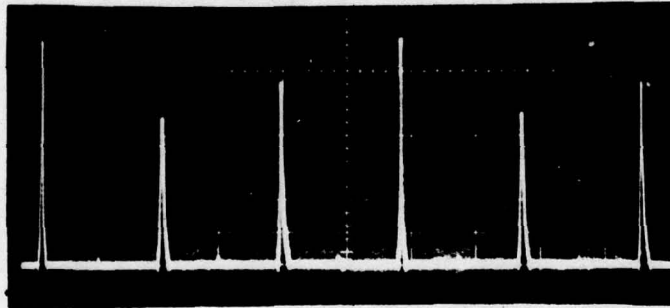


THYRISTOR VOLTAGE 100V/DIV. 200μSEC/DIV.

MAXIMUM FORWARD VOLTAGE = 300V

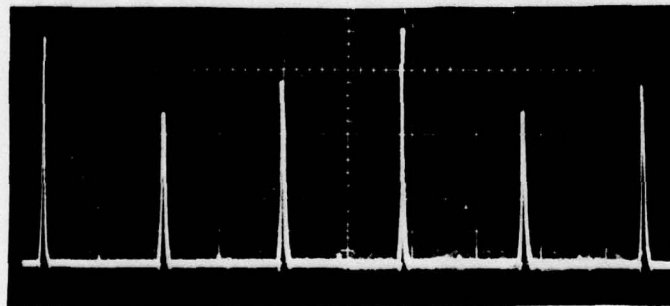
SELECT 600V THYRISTOR. REV. TURN-OFF TIME 80μSEC.

SELECT 40μSEC TURN-OFF TIME THYRISTOR.



1 P.U. LOAD

FREQUENCY = 1080 Hz



2.5 P.U. LOAD

THYRISTOR CURRENTS 300A/DIV. 500μSEC/DIV.

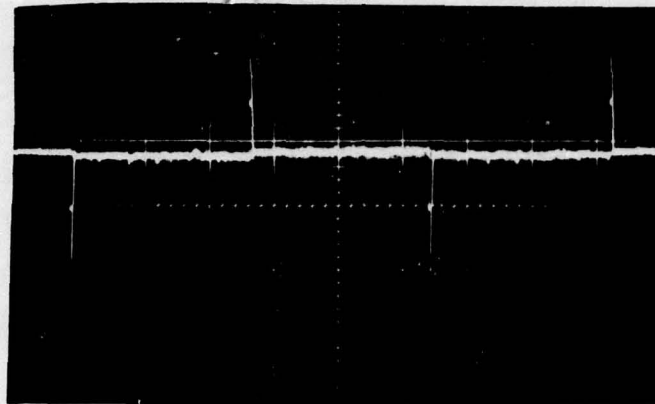
PEAK CURRENT = 1100A.

DUTY CYCLE = 0.1

SELECT (W) T727063544DN 77.59

(600V, 350A. AVG. 4μSEC)

TC<sup>+</sup>, TC<sup>-</sup> THYRISTORS

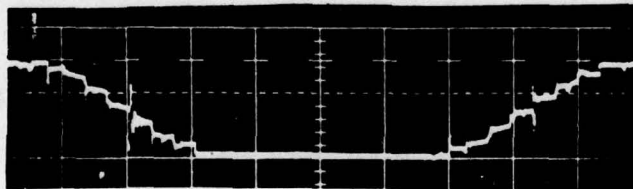


THYRISTOR VOLTAGE 300V/DIV. 1MS/DIV.

PEAK FORWARD VOLTAGE = 750V. SELECT 1000V. THYRISTOR.

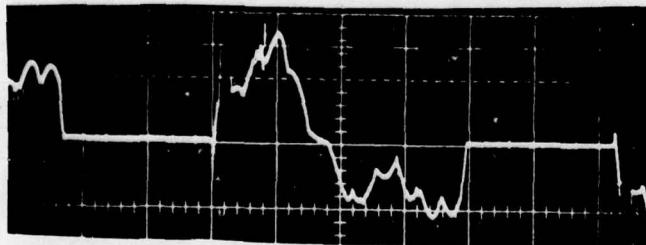
Ⓜ TS07107064 (1000V, 70A. AVG. 20  $\mu$ SEC.) \*59.78

BY-PASS DIODES



DIODE VOLTAGE 300V/DIV. 400  $\mu$ S

PEAK DIODE VOLTAGE = 450V.  
SELECT 800V. DIODE



↑ THYRISTOR CURRENT

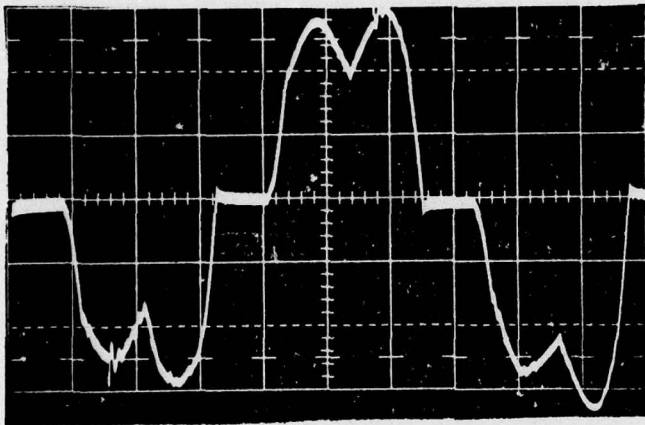
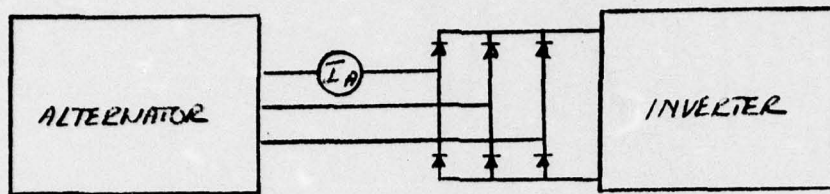
0

↓ DIODE CURRENT

CURRENT 300A/DIV. DUTY CYCLE = 0.10 AVG. DIODE CURRENT = 50A.  
PEAK DIODE CURRENT DURING COMMUTATION = 1260A.

· SELECT Ⓜ R5020810 FJ (800V, 100A. AVG. FAST REC.) \*18.70

## RECTIFIER DIODES



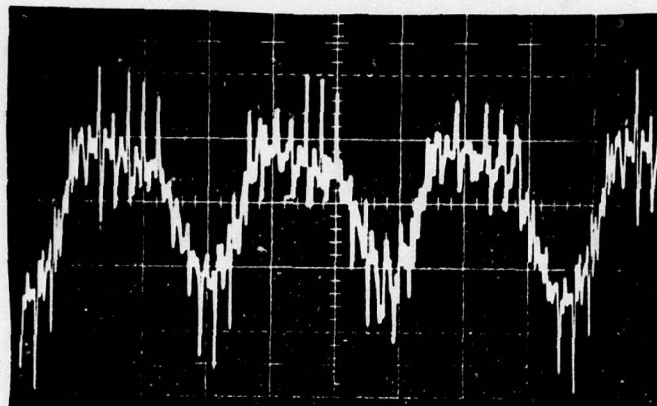
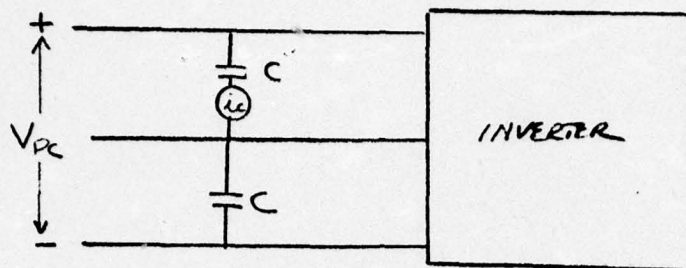
DIODE CURRENT 120A/DIV. 100μSEC/DIV.  
FREQUENCY = 1600Hz 1 P.U. LOAD

MAXIMUM CURRENT FOR 1 P.U. LOAD = 360 A.  
MAXIMUM CURRENT FOR 2.5 P.U. LOAD = 900 A.

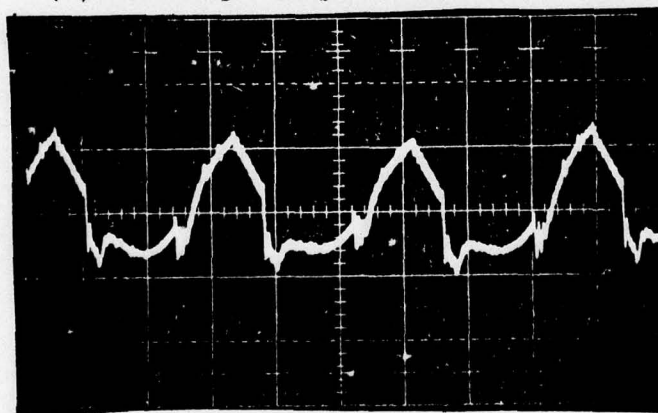
AVG. DIODE CURRENT = 300 A. FOR 2.5 P.U. LOAD.

SELECT (W) R62Z1035 FT (350A AVG. 1000V.) FAST  
RECOVERY DIODE, \$25.50

# INPUT FILTER CAPACITOR



1 P.U. LOAD 300 A RMS



2.5 P.U. LOAD 192 A RMS

CAPACITOR CURRENT  $i_C$ ; 300A/DIV. 2MS/DIV.  
60Hz

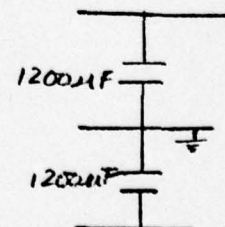
2 P.U. CAPACITOR CURRENT = 600A RMS

REQUIRES 12 CAPACITORS RATED AT 50A RMS.

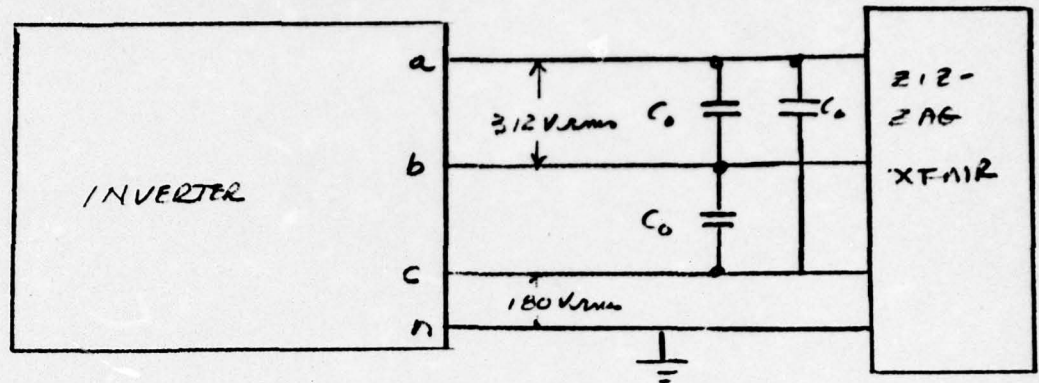
$V_{DC} = 450VDC$ .

SELECT SPRAGUE TYPE 331P METALLIZED PAPER DIELECTRIC CAPACITORS: 400VDC 100μF (12 PER SECTION)

TYPE 331P 400VDC 100μF COST \$40 EACH. TOTAL COST \$480.



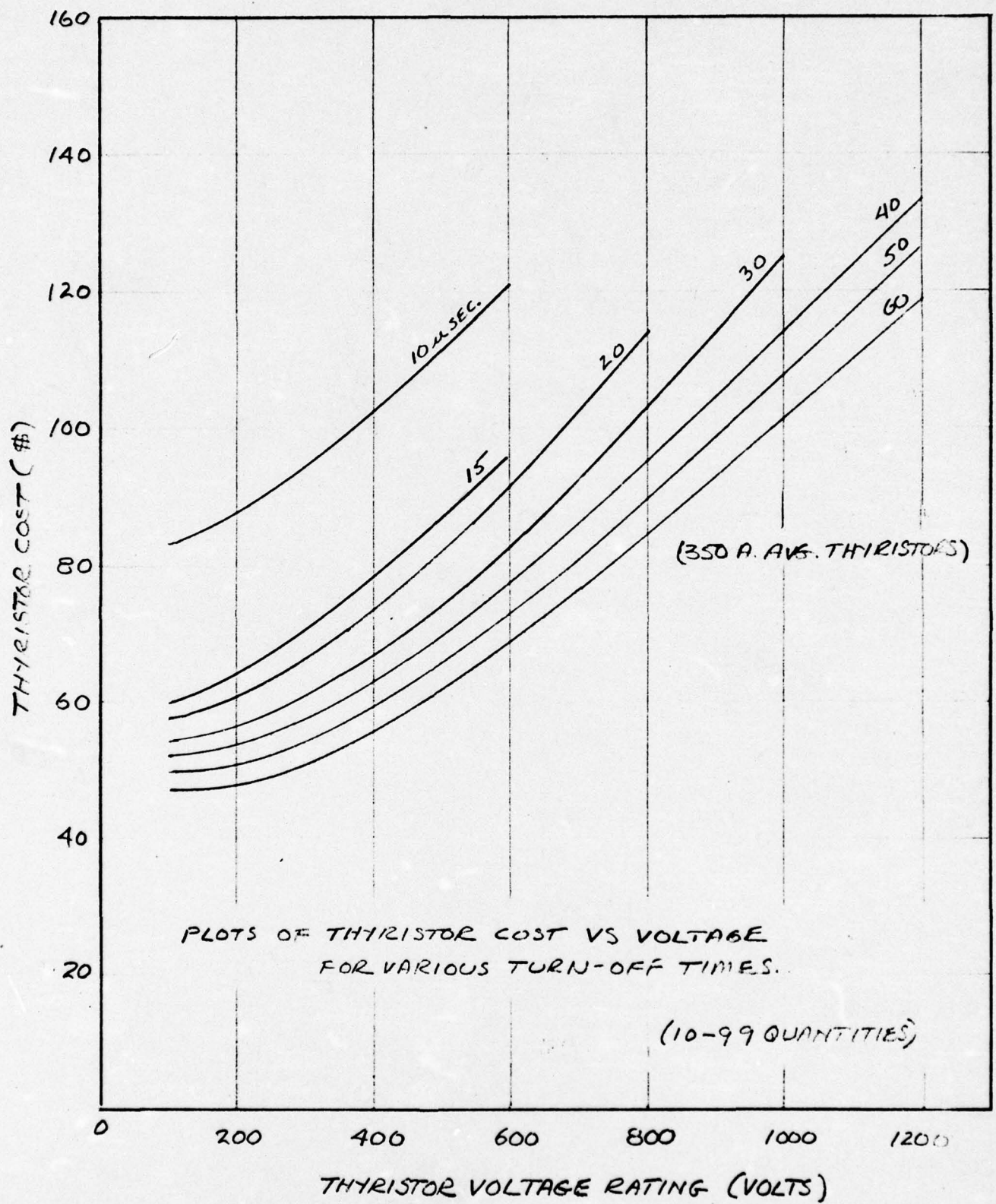
## OUTPUT FILTER CAPACITOR

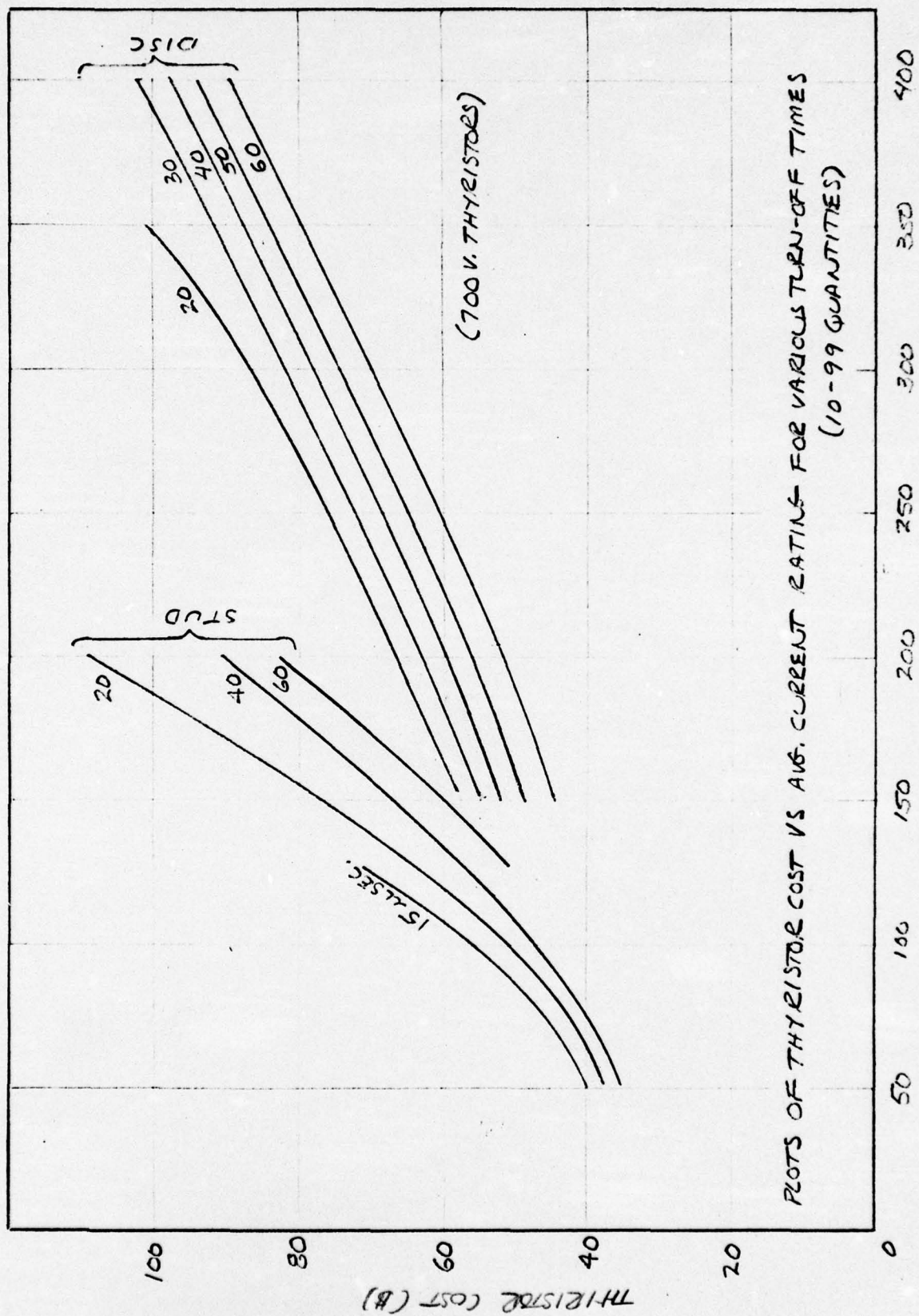


MERDC BREADBOARD MODEL -  $C_0 = 60 \text{ MFD}$  REQUIRED  
ACROSS 208 Vrms L-T-L TO PRODUCE 20 KW, 0.8 PF  
LOAD AT 400 Hz, P.F. CORRECTED MODE OF  
OPERATION, FIVE TIMES MULTIPLIER REQUIRED  
FOR 100 KW, 0.8 PF TIMES  $\frac{208}{312}$  VOLTAGE RATIO MULTIPLIER.

REQUIRED L-T-L OUTPUT FILTER CAPACITANCE  
FOR 100 KW INVERTER =  $(60) \left( 5 \left( \frac{208}{312} \right) \right) = \underline{\underline{200 \text{ MFD}}}$

SELECT SPRAGUE TYPE 330 PAPER DIELECTRIC  
CAPACITOR 50  $\mu\text{F}$ , 600 V DC, 100 V RMS (330 PBJ).  
FOUR (4) CAPACITORS REQUIRED PER PHASE OR  
TWELVE (12) TOTAL. COST OF OUTPUT FILTER  
AT \$1/MFD = \$600.

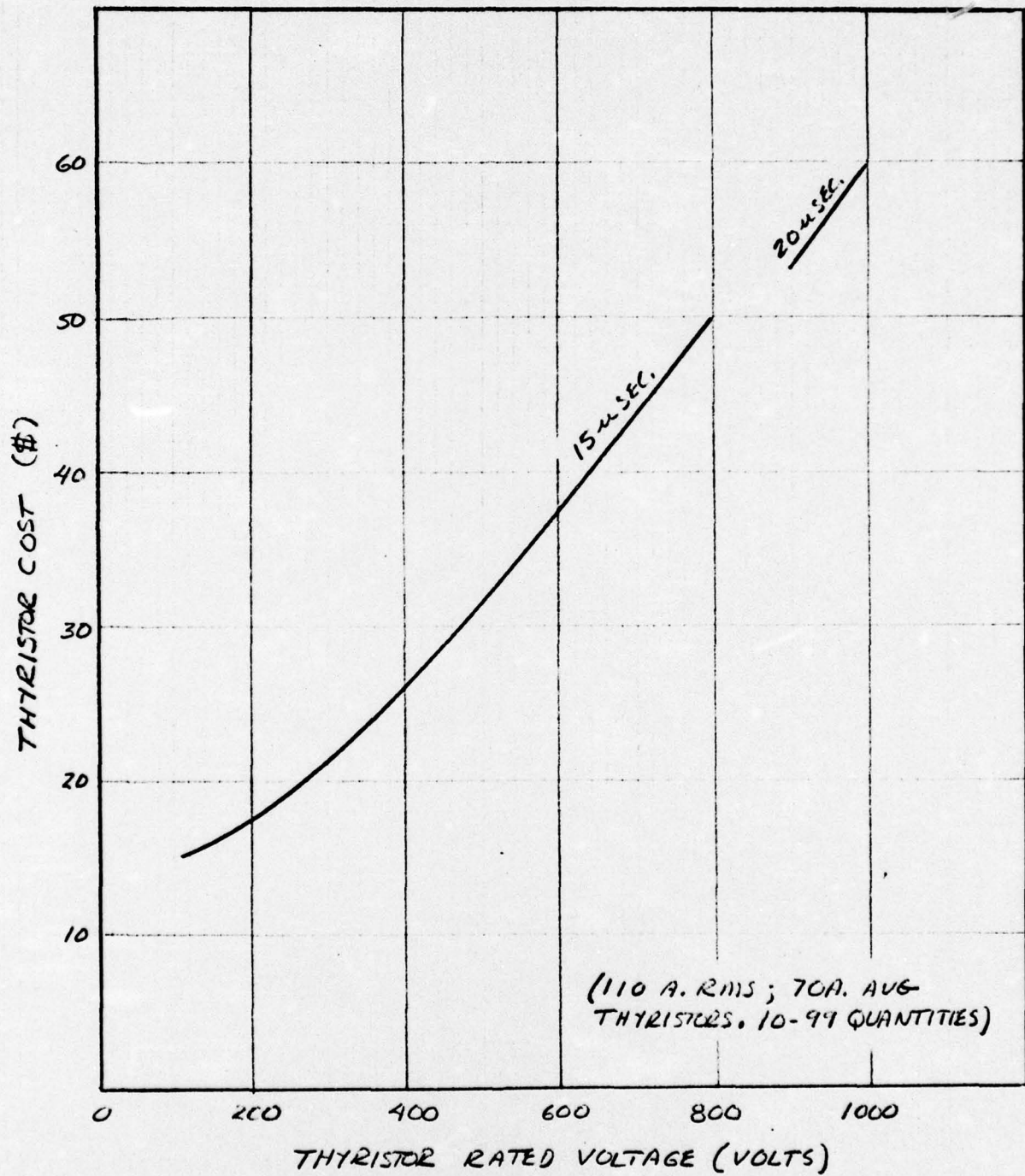




PLOTS OF THYRISTOR COST VS. AVG. CURRENT RATING FOR VARIOUS TURN-OFF TIMES  
(10-99 QUANTITIES)

THYRISTOR AVG. CURRENT RATING (AMPERES)

PLOTS OF THYRISTOR COST VS VOLTAGE FOR 15 & 20  $\mu$ SEC,  
TURN-OFF TIMES



**TASK 3**

**Design and Test Data**  
**Final Technical Report**  
**Sequence A002**

TITLE

PREPARED

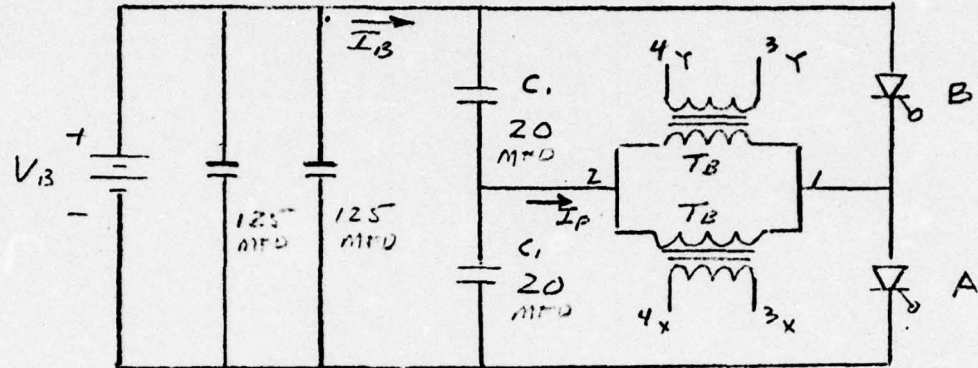
CORRY 5/5/75

DATE

CHECKED

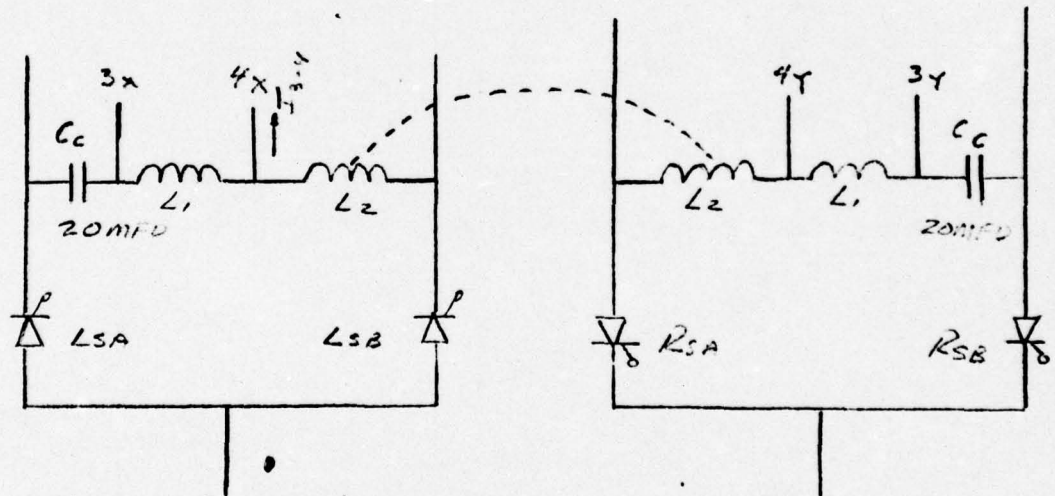
APPROVED

# COMMUTATION BOOST CIRCUIT VOLTAGE AND CURRENT WAVEFORMS (60 HZ OPERATION)



X STEPS

Y STEPS



	$V_{RMS}$	$I_{RMS}$
$C_1$	100	32
$C_2$	135	50

$$V_B = 66 \text{ VDC}$$

$$I_P = 9 \text{ AMPS DC}$$

$$V_{2,4} = 14.2 \text{ V RMS}$$

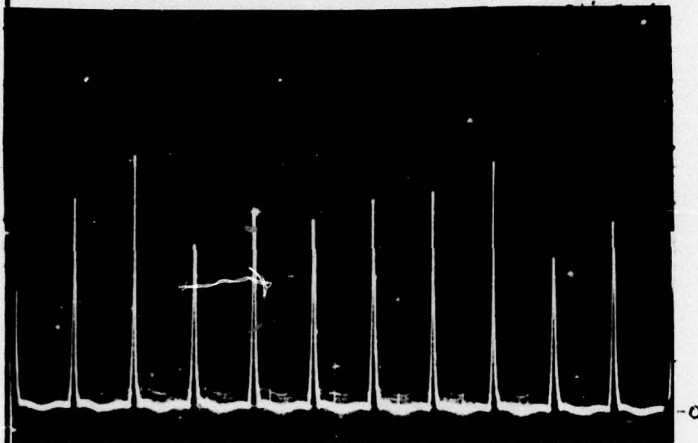
$$I_{2,4} = 67 \text{ A RMS}$$

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CORY  
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APPROVED  
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5/5/75

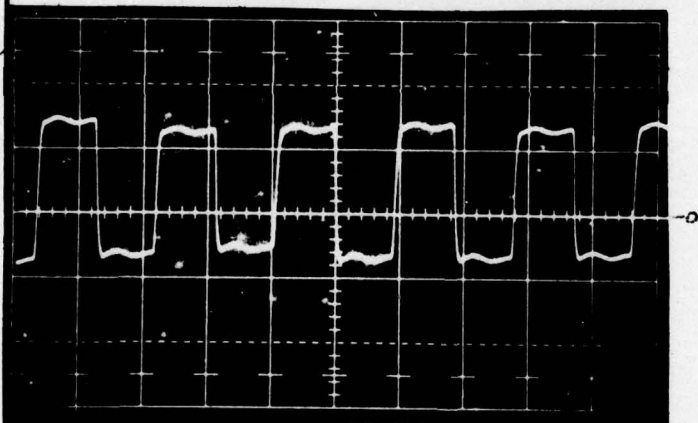
COMMUTATION BOOST CIRCUIT VOLTAGE  
AND CURRENT WAVEFORMS



$I_B$

50 A/DIV.

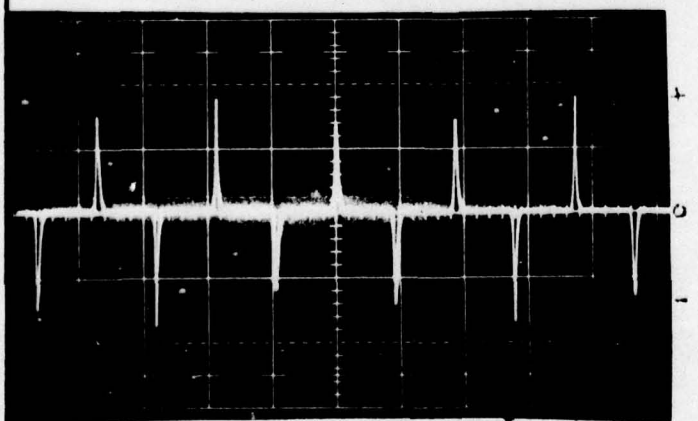
500  $\mu$ SEC/DIV.



VOLTAGE ACROSS  
A C, CAPACITOR

100V/DIV.

500  $\mu$ SEC/DIV.



CURRENT INTO  
PRIMARIES OF  
TRANSFORMERS  $T_B$

200 A/DIV. 500  $\mu$ SEC/DIV.

B CURRENTS  $\uparrow$   
A CURRENTS  $\downarrow$

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REPORT NO.

ITEM NO.

0009

PAGE

JOB NO.

DESIGN

DATA

PAGE

3

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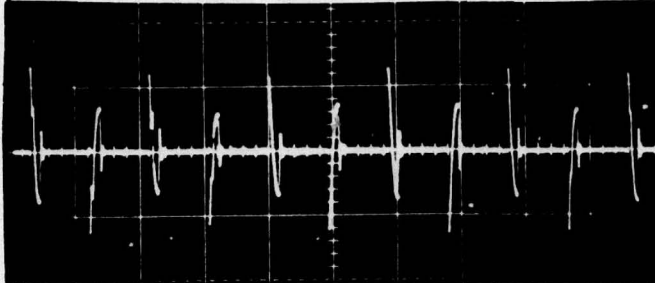
CORY

DATE

5/5/75

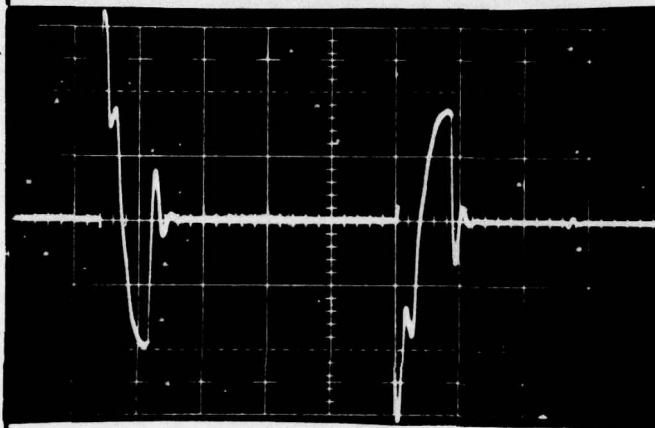
CHECKED

APPROVED

BOOST CIRCUIT WAVEFORMSVOLTAGE ACROSS L<sub>1</sub>

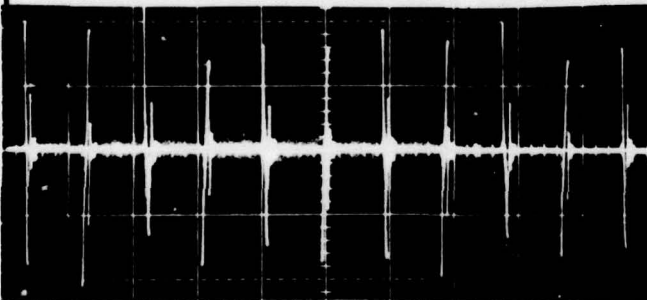
50V/DIV.

500μSEC/DIV.



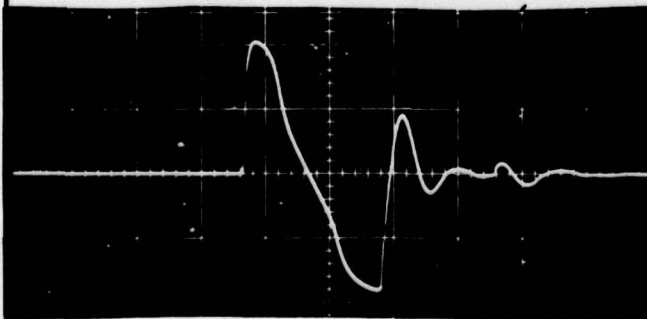
20V/DIV.

100μSEC/DIV.

VOLTAGE ACROSS L<sub>2</sub>

50V/DIV.

500μSEC/DIV.



20V/DIV.

100μSEC/DIV.

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REPORT NO.

ITEM NO.  
0009

PAGE

JOB NO.

DESIGN  
DATA

PAGE

4

TITLE

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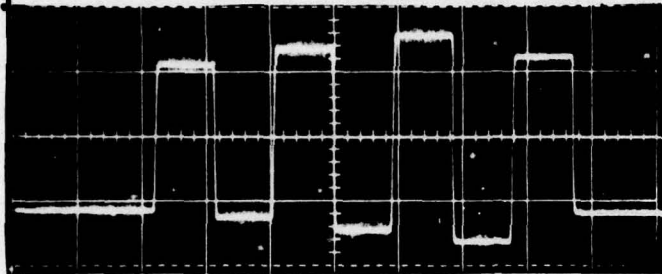
DATE

5/5/75

CHECKED

APPROVED

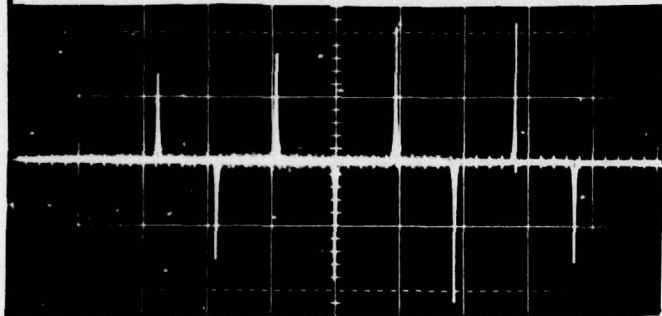
# BOOST CIRCUIT WAVEFORMS



VOLTAGE ACROSS  $C_c$

50V/DIV.

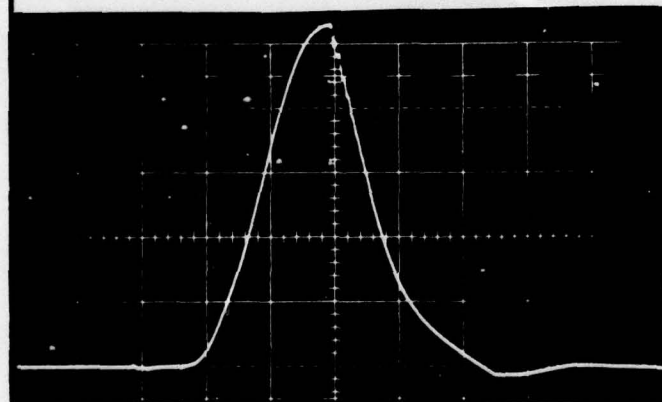
500  $\mu$ SEC/DIV



CURRENT THRU  $C_2$

200A/DIV.

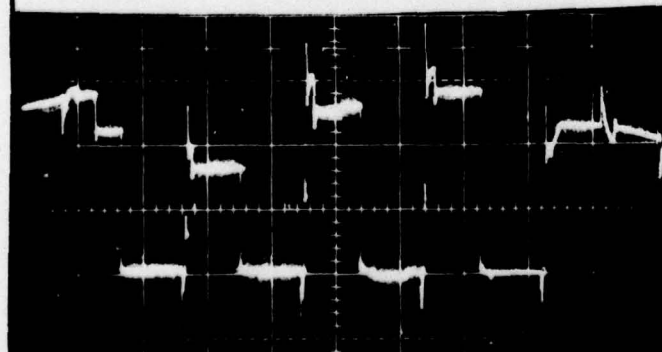
500  $\mu$ SEC/DIV



CURRENT THRU  $C_2$

50A/DIV

10  $\mu$ SEC/DIV.



VOLTAGE ACROSS  $L_{SA}$

50V/DIV.

500  $\mu$ SEC/DIV.

11KW, PF = 0.8

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REPORT NO.  
ITEM NO.  
0009PAGE  
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DESIGN  
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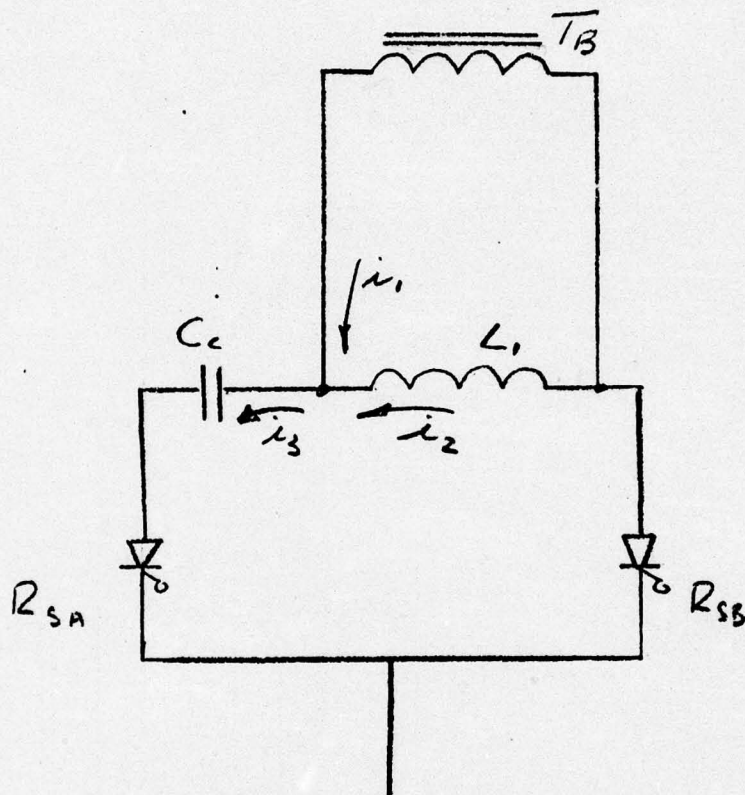
CORRY

DATE

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BOOST CIRCUIT WAVEFORMS

DISTRIBUTION:

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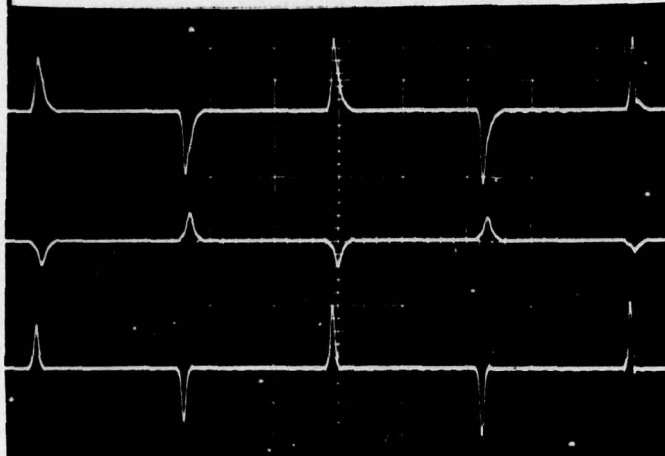
CORY

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2

1

0

1

2

STEP NUMBER

COMMUTATION CURRENT WAVEFORMS $i_1$ UNCALIBRATED  
CURRENT SCALE $i_2$ 200  $\mu$ SEC / DIV. $i_3$ 0 INPUT VOLTAGE  
TO INVERTER

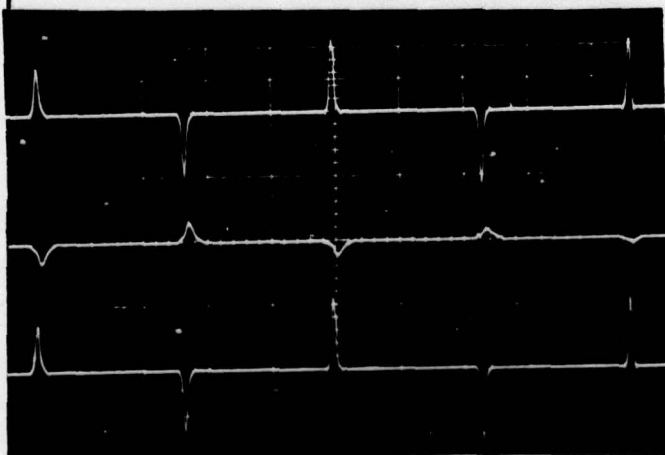
2

1

0

1

2

 $i_1$ 290 VDC INPUT  
VOLTAGE $i_2$ NO LOAD $i_3$ 

2

1

0

1

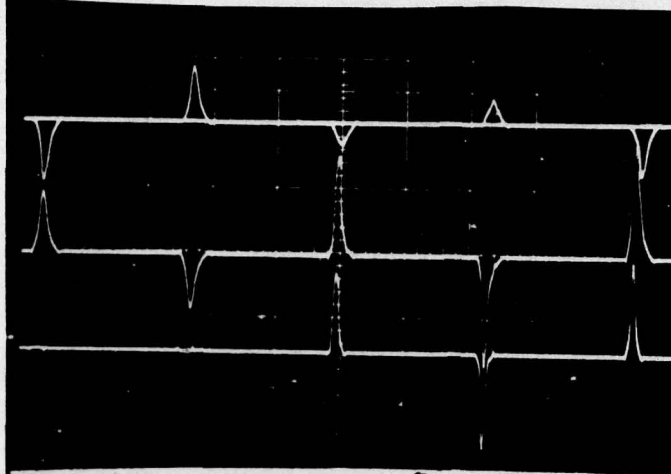
2

 $i_1$ 294 VDC INPUT  
VOLTAGE $i_2$ 11KW, 0.8 PF LOAD $i_3$ (THREE WIRE INPLT.  
 $V_{1300ST} = 66VDC; I_B = 8A.$ )  
FOR PAGES 1-13

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	PREPARED CORRY 5/5/75 CHECKED APPROVED		
TITLE			

# COMMUTATION CURRENT WAVEFORMS



$i_1$

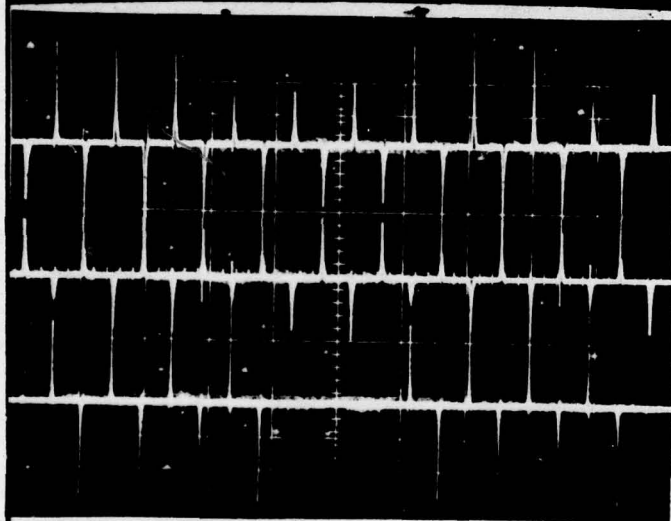
0 INPUT VOLTAGE

$i_2$

200A/DIV

$i_3$

200μSEC/DIV



$i_1$

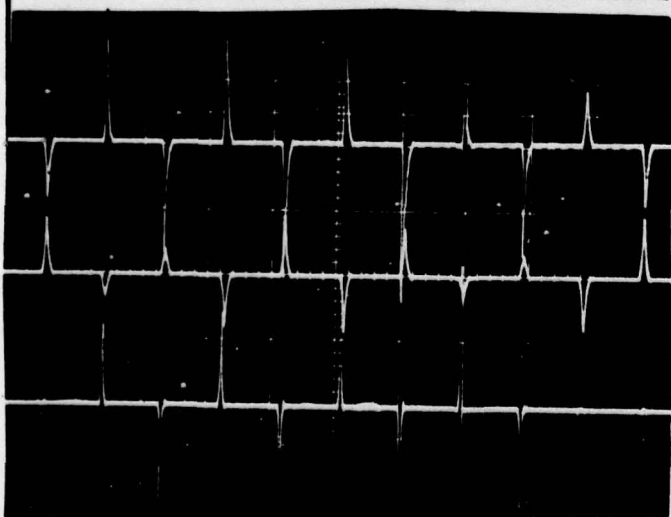
0 INPUT VOLTAGE

$i_2$

200A/DIV

$i_3$

1MS/DIV



$i_1$

0 INPUT VOLTAGE

$i_2$

200A/DIV

$i_3$

500μSEC/DIV

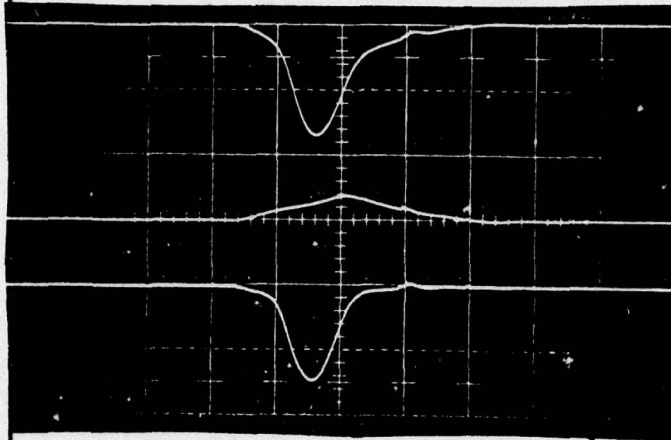
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PC 3 2 1 0 1 2 3 STEP NO.

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COMMUTATION CIRCUIT WAVEFORMS



$i_1$

$R_3$  SHUT-OFF TIME

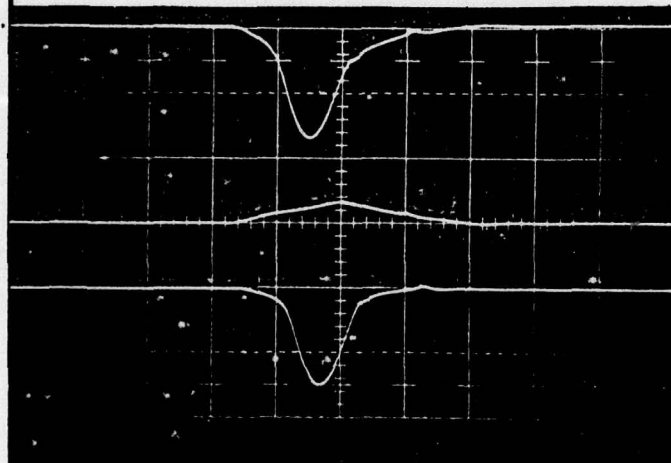
200A / DIV

20  $\mu$ SEC / DIV.

$i_2$

0 INPUT VOLTAGE

$i_3$



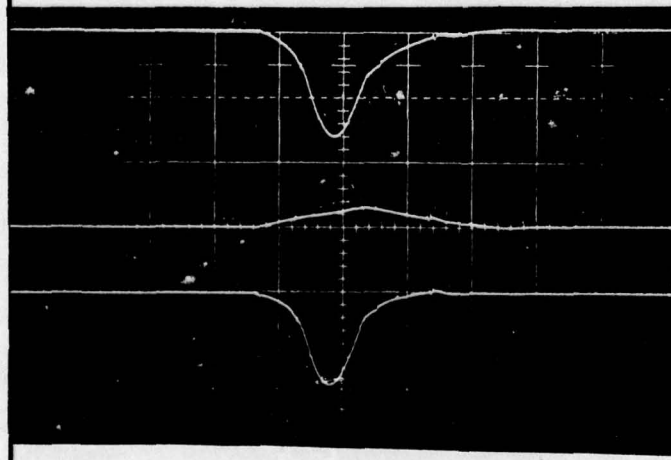
$i_1$

291VDC INPUT VOLTAGE

NO LOAD

$i_2$

$i_3$



$i_1$

294VDC INPUT

11KW, 0.8PF LOAD

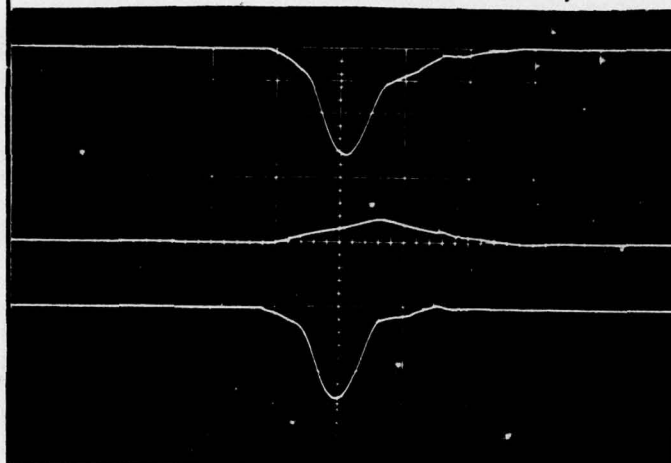
$i_2$

$i_3$

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	TITLE		PREPARED CORRY 5/5/75	DATE
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# POST CIRCUIT WAVEFORMS

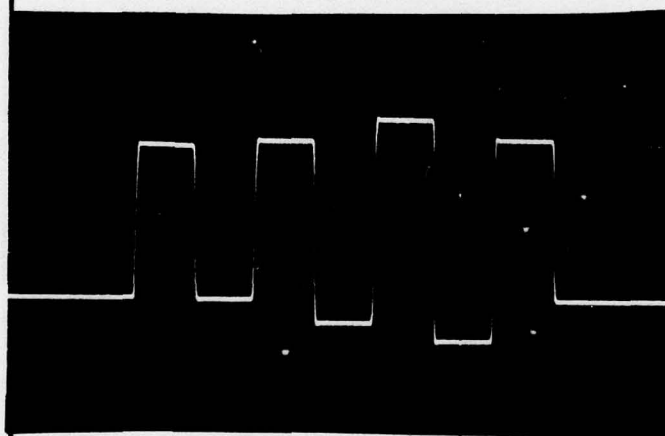


## R<sub>2</sub> SHUT-OFF TIME

200A / DIV.  
20 μSEC / DIV.

SHORT CKT 3φ  
L-T-N

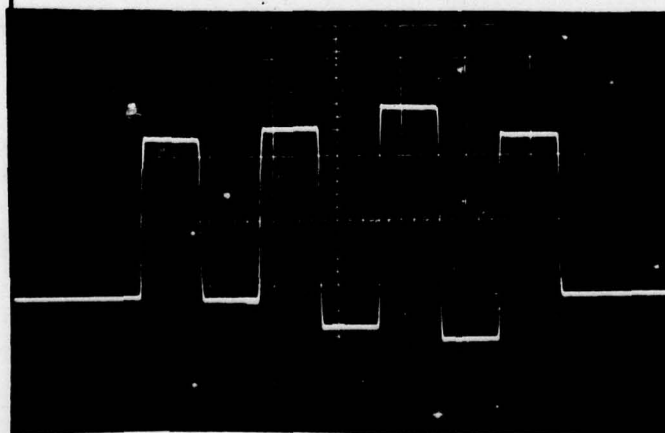
V<sub>α</sub> = 13.5VDC  
I<sub>α</sub> = 95ADC



## VOLTAGE ACROSS C<sub>c</sub>

100V / DIV  
500 μSEC / DIV.

## 0 INPUT VOLTAGE



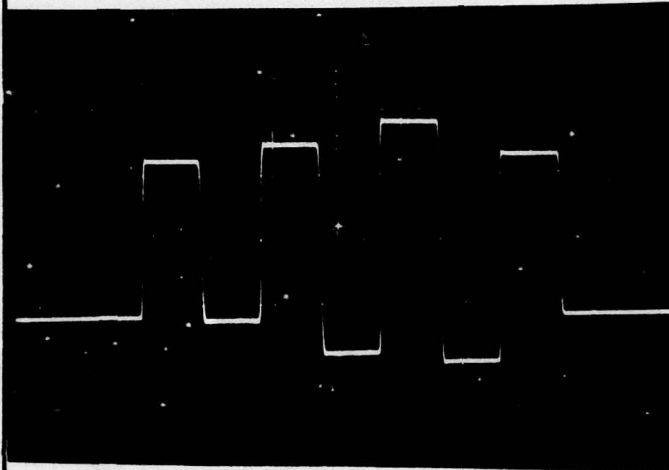
291VDC INPUT VOLTAGE  
NO LOAD

DISTRIBUTION:

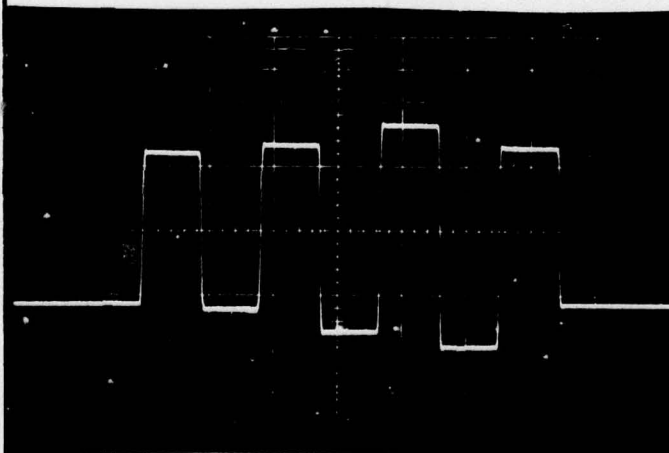
TITLE

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APPROVED

BOOST CIRCUIT WAVEFORMS



294VDC INPUT VOLTAGE  
11KΩ, 0.8PF LOAD



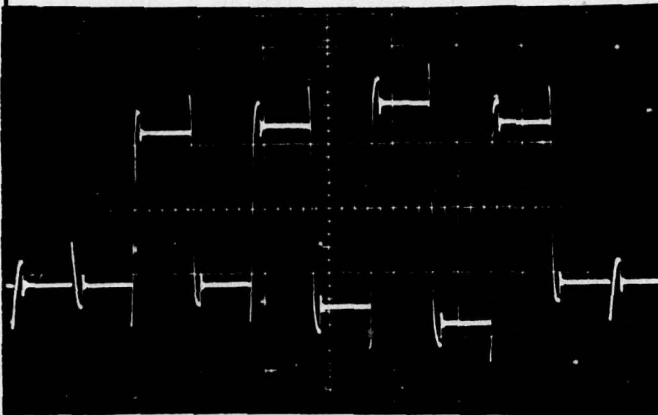
SHORT CKT 30  
L-T-N

13.6VDC INPUT VOLTAGE  
95A DC INPUT CURRENT

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	TITLE		PREPARED CORRY	DATE 5/5/75
		CHECKED		
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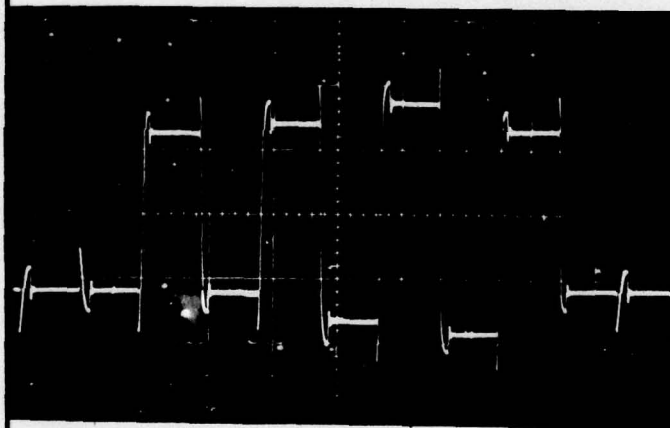
# BOOST CIRCUIT WAVEFORMS



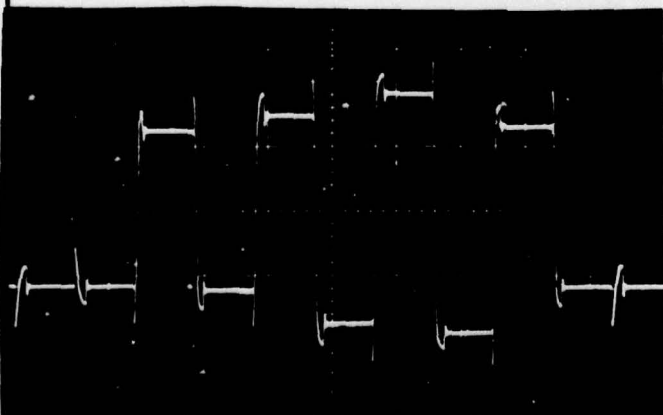
TOTAL TURN OFF VOLTAGE  
 $V_{cc} + V_L$

100V / DIV.  
500  $\mu$ SEC / DIV.

0 INPUT VOLTAGE



291 VDC INPUT VOLTAGE  
NO LOAD



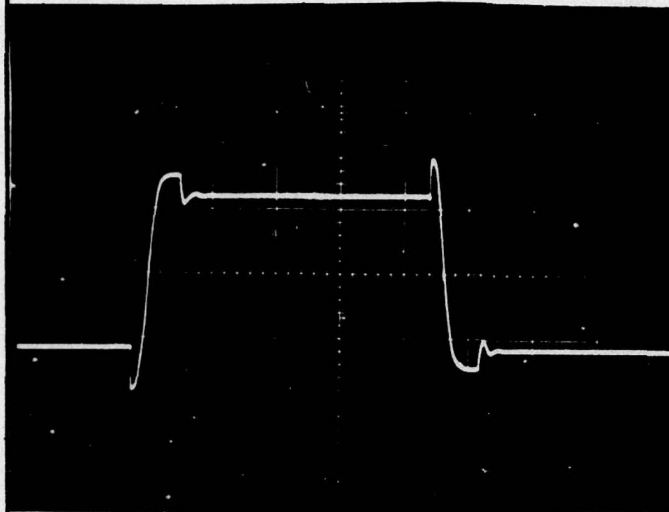
299 VDC INPUT VOLTAGE  
11 KW, 0.8 PF LOAD

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CORRY 5/5/75  
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APPROVED

BOOST CIRCUIT WAVEFORMS



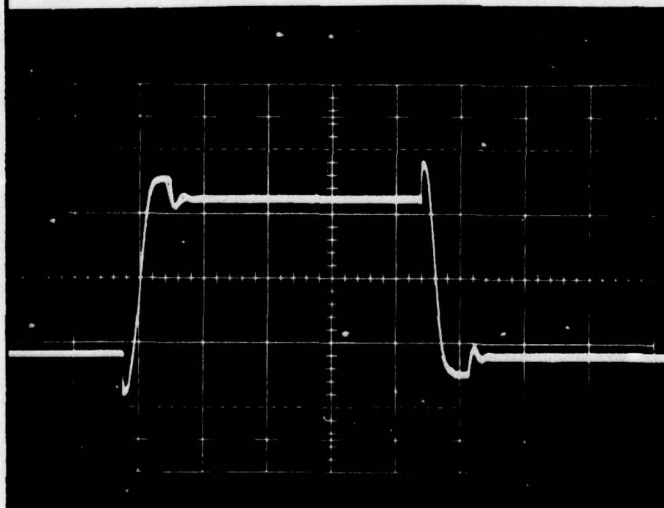
P.C. TURN-OFF

R<sub>3</sub> TURN-OFF

TOTAL TURN OFF VOLTAGE  
 $V_{CC} + V_L$

R<sub>3</sub> TURN OFF TIME  
100V/DIV.  
100μSEC/DIV.

0 INPUT VOLTAGE



TRIPLE EXPOSURE

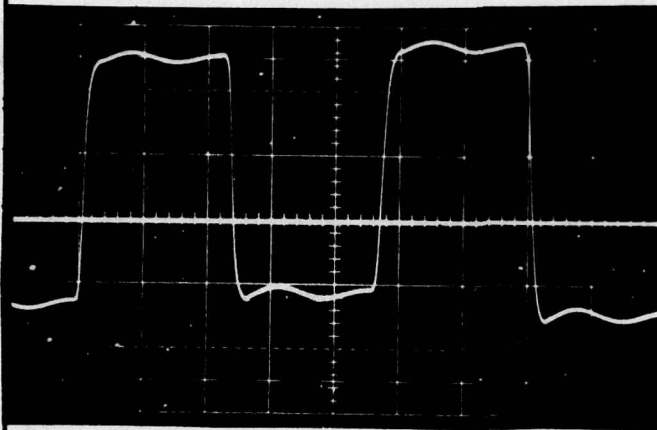
- 1) 0 INPUT VOLTAGE
- 2) 291VDC INPUT VOLTAGE  
NO LOAD
- 3) 294VDC INPUT VOLTAGE  
11KW, 0.8PF LOAD

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CHECKED  
APPROVED

BOOST CIRCUIT WAVEFORMS

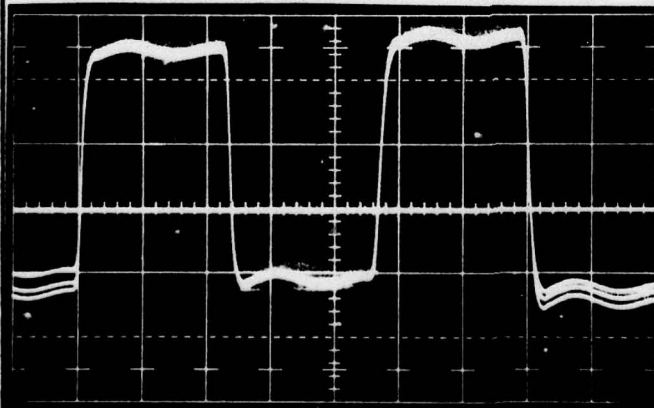


VOLTAGE ACROSS  
A C, CAPACITOR

50V / DIV.

200μSEC / DIV.

0 INPUT VOLTAGE



TRIPLE EXPOSURE

- 1) 0 INPUT VOLTAGE
- 2) 290 VDC INPUT VOLTAGE  
NO LOAD
- 3) 294 VDC INPUT VOLTAGE  
11KW, 0.8PF LOAD

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REPORT NO.

ITEM NO.

0009

PAGE

JOB NO.

DESIGN

DATA

PAGE

14

TITLE

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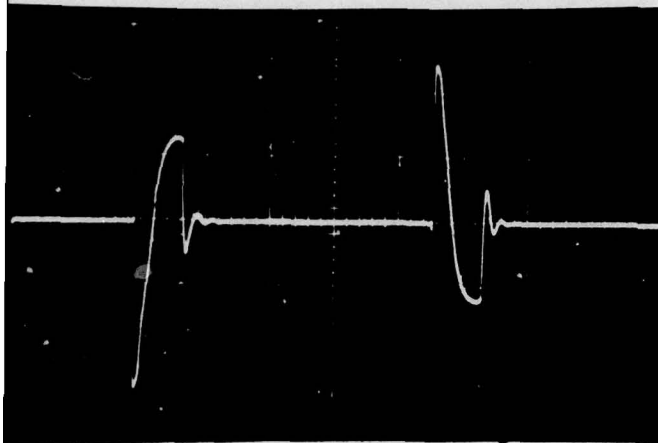
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# BOOST CIRCUIT WAVEFORMS

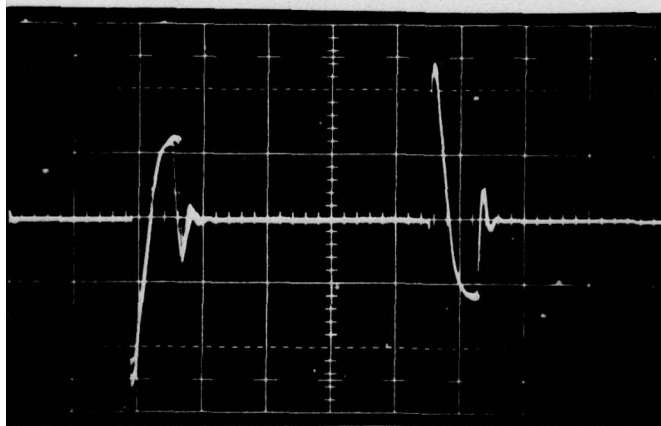


VOLTAGE ACROSS PRIMARY  
OF BOOST TRANSFORMERS

50V/DIV.

100 μSEC/DIV.

0 INPUT VOLTAGE



TRIPLE EXPOSURE

- 1) 0 INPUT VOLTAGE
- 2) 290 VDC INPUT VOLTAGE  
NO LOAD
- 3) 294 VDC INPUT VOLTAGE  
11KW, 0.8 PF LOAD

TITLE

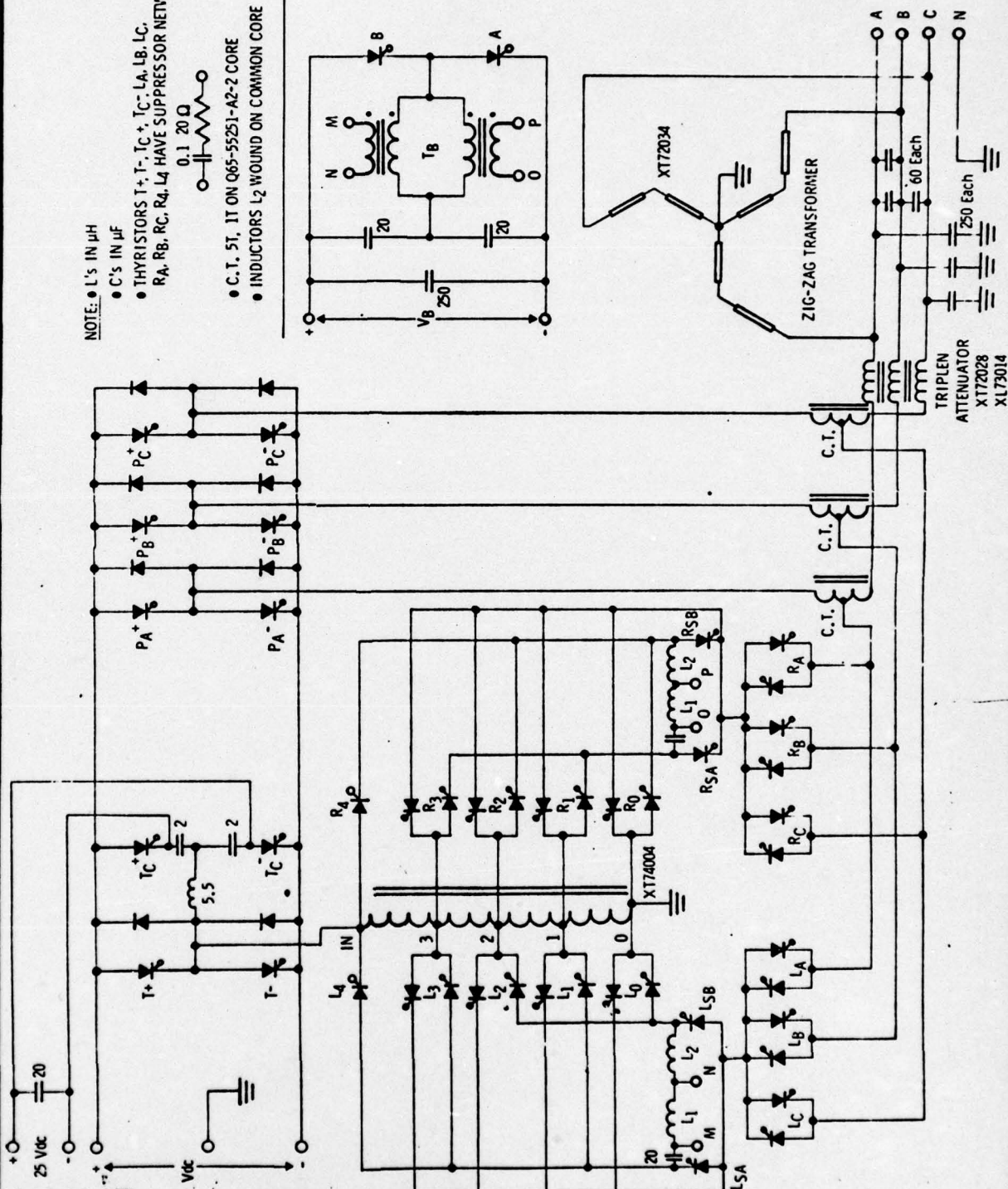
PREPARED  
CORRY 5/5/75

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APPROVED

# THYRISTOR AND DIODE VOLTAGES AND CURRENTS

- NOTE: ● L's IN  $\mu$ H  
● C's IN  $\mu$ F  
● THYRISTORS T<sup>+</sup>, T<sup>-</sup>, T<sub>C</sub>, T<sub>C</sub><sup>+</sup>, L<sub>A</sub>, L<sub>B</sub>, L<sub>C</sub>,  
R<sub>A</sub>, R<sub>B</sub>, R<sub>C</sub>, R<sub>A</sub>, L<sub>4</sub> HAVE SUPPRESSOR NETWORKS:  
0.1 20  $\Omega$   
● C.T., 5T, 1T ON Q65-55251-A2-2 CORE  
● INDUCTORS L<sub>2</sub> WOUND ON COMMON CORE



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GENERAL MOTORS CORPORATION

REPORT NO.

ITEM NO.

0009

PAGE

JOB NO.

DESIGN

DATA

PAGE

16

TITLE

PREPARED

CORRY

DATE

5/5/75

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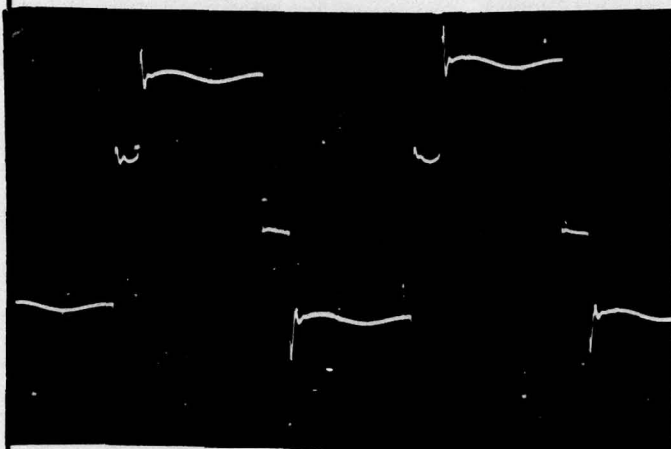
THYRISTOR VOLTAGES 60Hz

CONDITIONS:

$V_{DC} = 300VDC$  INPUT VOLTAGE

$V_{BOOST} = 66VDC$ ;  $I_B = 8$  AMPS.

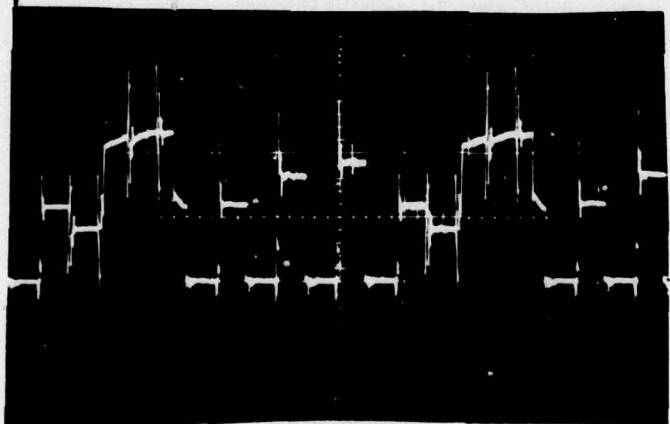
NO LOAD; 60MFD. L-TL.



(A)

50V/DIV

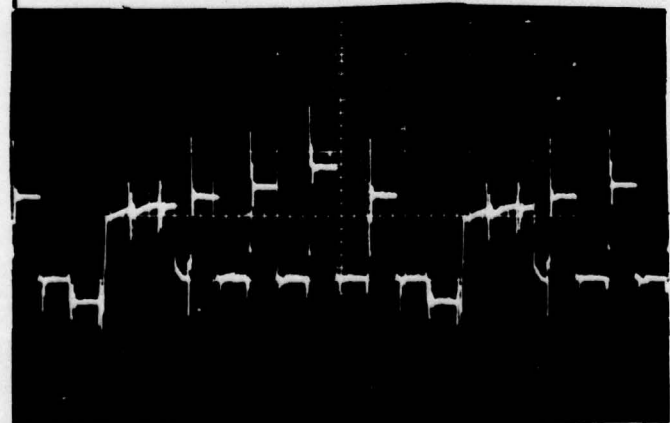
200μSEC/DIV.



(2SA)

100V/DIV.

1MS/DIV.



(2SB)

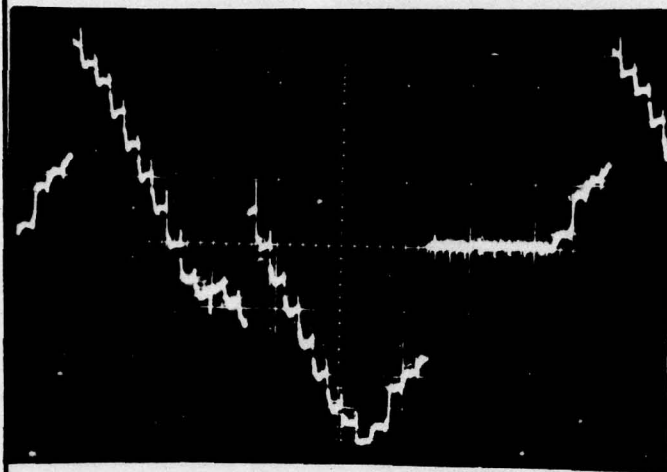
100V/DIV.

1MS/DIV.

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	TITLE		PREPARED CORY	DATE 5/5/75
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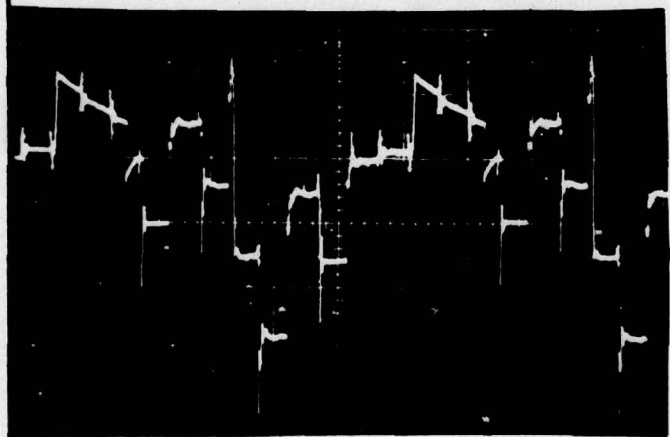
THYRISTOR VOLTAGES 60Hz



(R1)

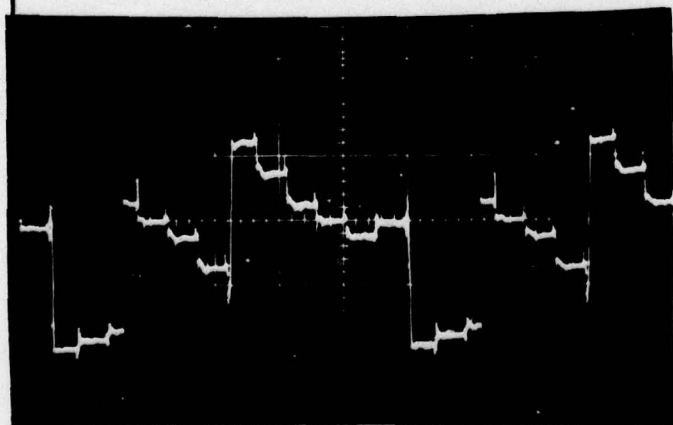
BACK-TO-BACK  
THYRISTORS

100V/DIV.  
2ms/DIV.



(R2)

100V/DIV  
1ms/DIV.



(R3)

FREE BUS

100V/DIV.  
1ms/DIV.

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GENERAL MOTORS CORPORATION

REPORT NO.

ITEM NO.

0009

PAGE

JOB NO.

DESIGN

DATA

PAGE

18

TITLE

PREPARED

CORRY 5/5/75

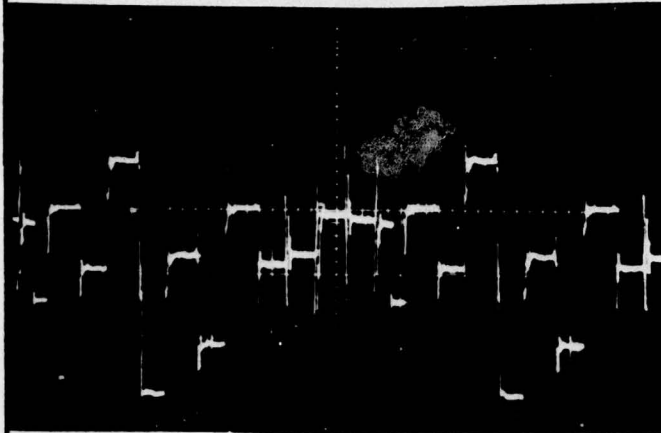
DATE

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THYRISTOR VOLTAGES

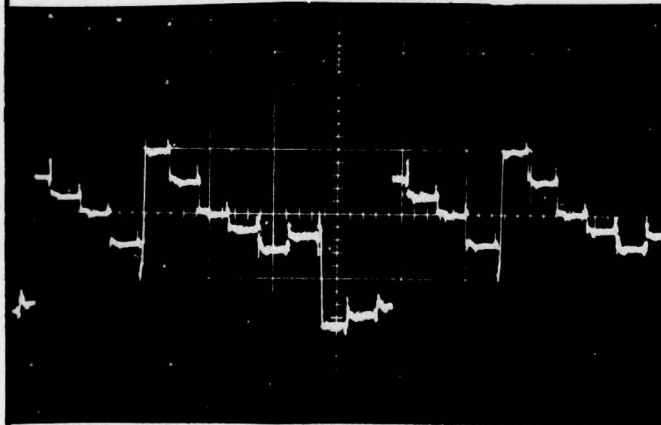
60HZ



(R3)

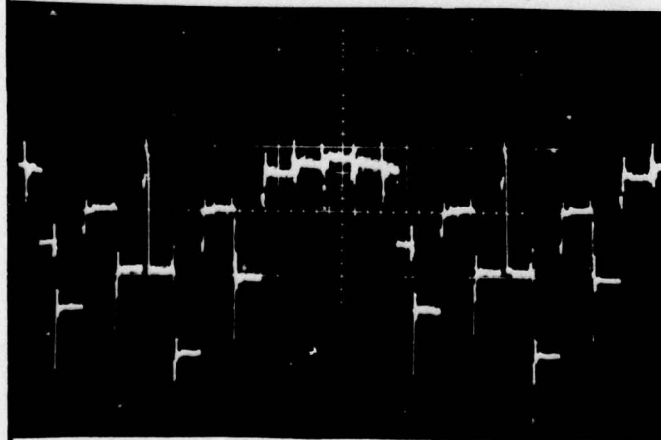
AUX. COMMUTATION

100V/DIV.  
1MS/DIV.



(R2)

FREE BUS



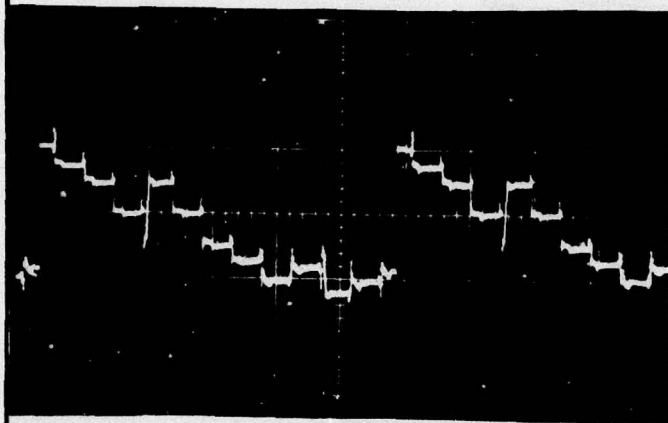
(R2)

AUX. COMMUTATION

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	TITLE		PREPARED CORRY 5/5/75	DATE
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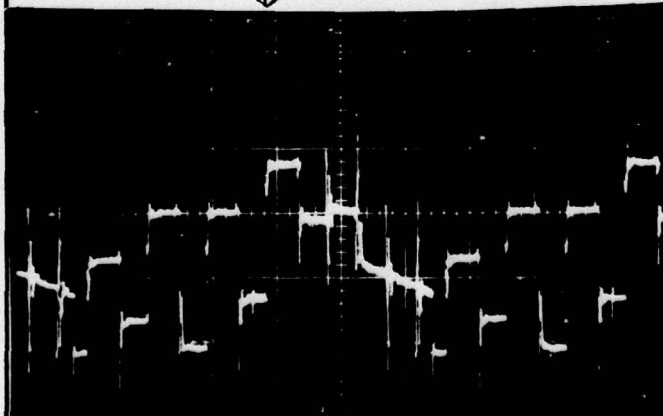
THYRISTOR VOLTAGES 60 HZ



(R<sub>1</sub>)  
FREE BUS

100V/DIV.  
1MS/DIV.

200V FORWARD VOLTAGE  
SPIKE  
↓

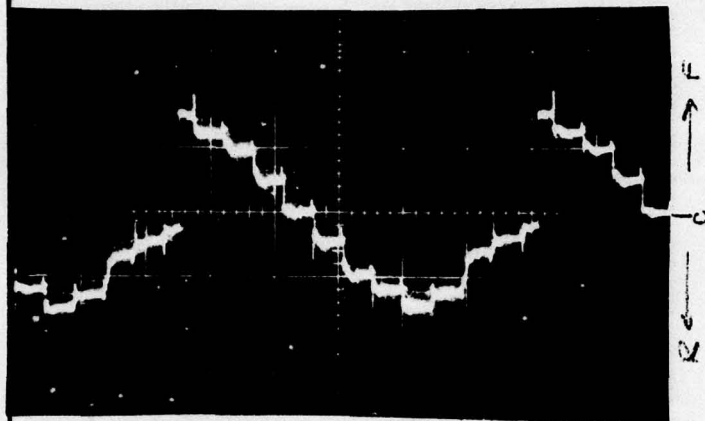


(R<sub>1</sub>)  
AUX. COMMUTATION

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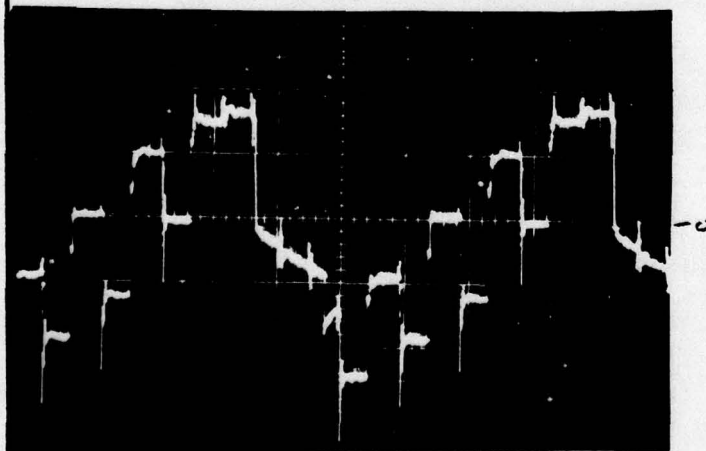
DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0009	PAGE JOB NO. DESIGN DATA	PAGE 20
	PREPARED CORRY 5/5/75		DATE
TITLE		CHECKED	
		APPROVED	

THYRISTOR VOLTAGES 60Hz



(R0)  
FREE BUS

100V/DIV.  
1MS/DIV.

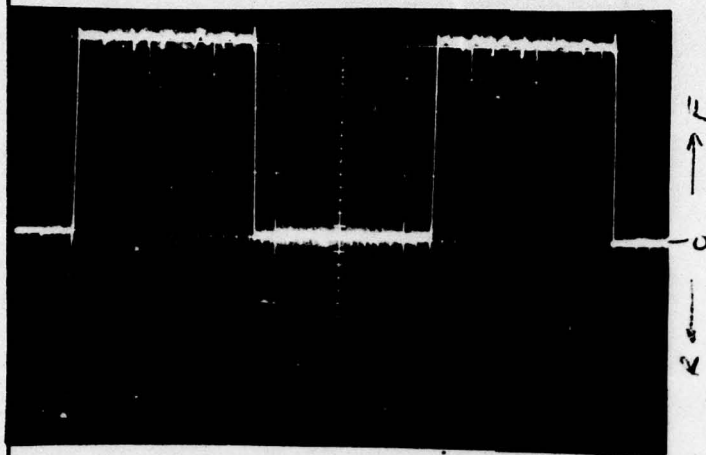


(R0)  
AUX. COMMUTATION

DISTRIBUTION:

DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0009	PAGE	JOB NO. DESIGN DATA	PAGE 21
	TITLE		PREPARED CORRY	DATE 5/5/75
		CHECKED		
		APPROVED		

# THYRISTOR VOLTAGES 60HZ

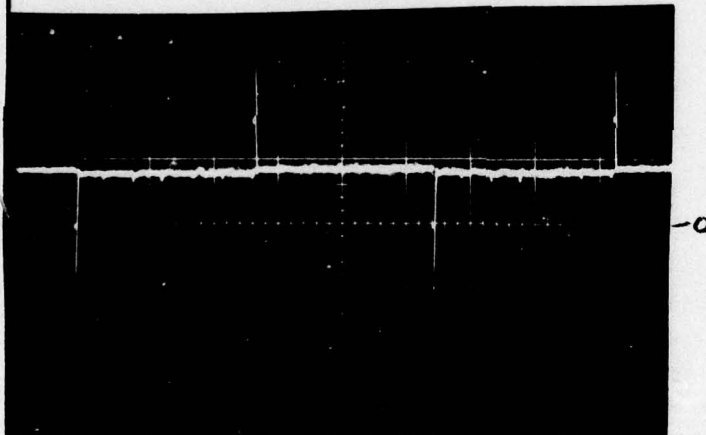


$T_+$  & DIODE

100V/DIV.

1MS/DIV.

(NO SPIKES LOADED  
OR NO LOAD)



$T_c+$

200V/DIV.

1MS/DIV.



$T_c+$

200V/DIV.

5μSEC/DIV.

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GENERAL MOTORS CORPORATION

REPORT NO.

ITEM NO.  
0009

PAGE

JOB NO.

DESIGN  
DATA

PAGE

22

TITLE

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CORRY

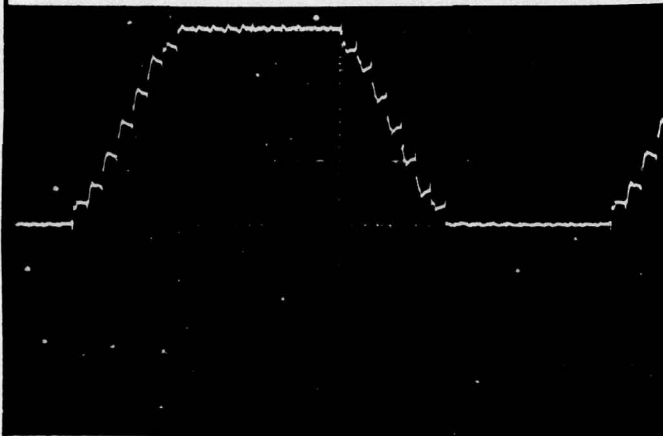
DATE

5/5/75

CHECKED

APPROVED

THYRISTOR VOLTAGES 60HZ



(P<sub>A</sub><sup>+</sup>) & DIODE

100V / DIV.

2ms / DIV.

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GENERAL MOTORS CORPORATION

REPORT NO.

ITEM NO.  
0009

PAGE

JOB NO.

DESIGN  
DATA

PAGE

23

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CORRY

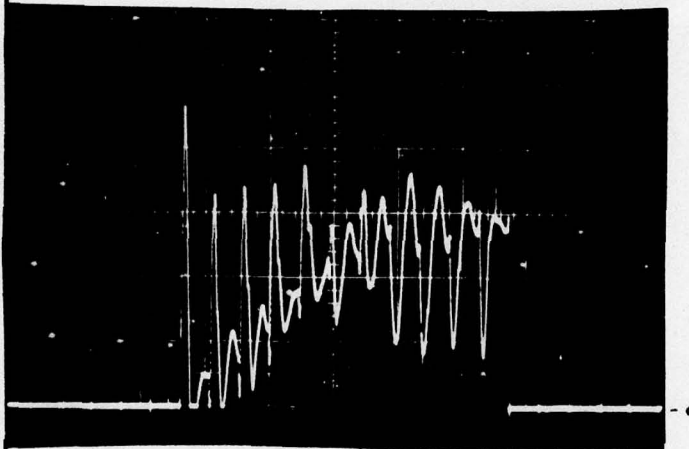
DATE

5-15-75

CHECKED

APPROVED

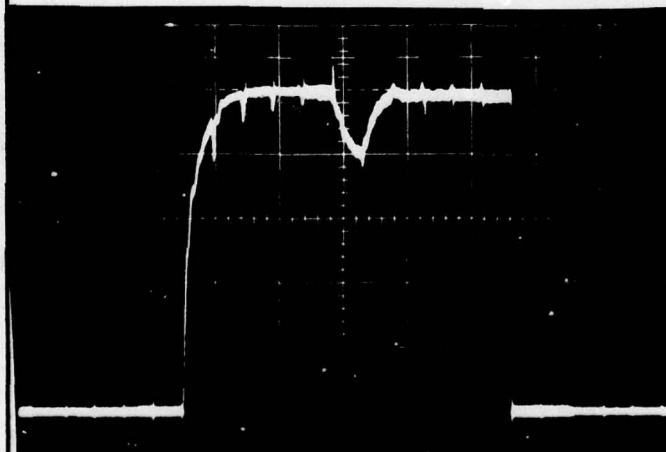
THYRISTOR CURRENTS 60 HZ



(P<sub>c</sub>)

20 A/DIV,  
1 MS/DIV.

11 KW, 0.8 PF LOAD



SHORT CIRCUIT  
3Φ, L-T-N

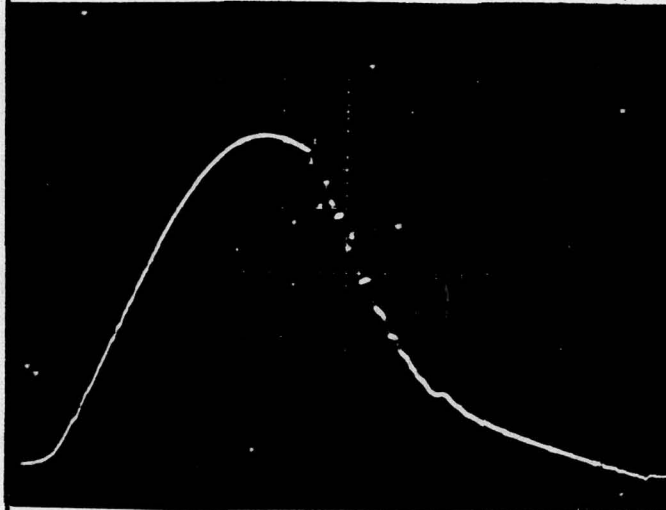
$V_{DC} = 13.5 \text{ VDC}$

$I_{DC} = 95 \text{ AMPS.}$

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	TITLE		PREPARED CORR/ 5/5/75	DATE
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		APPROVED		

THYRISTOR CURRENTS 60 Hz

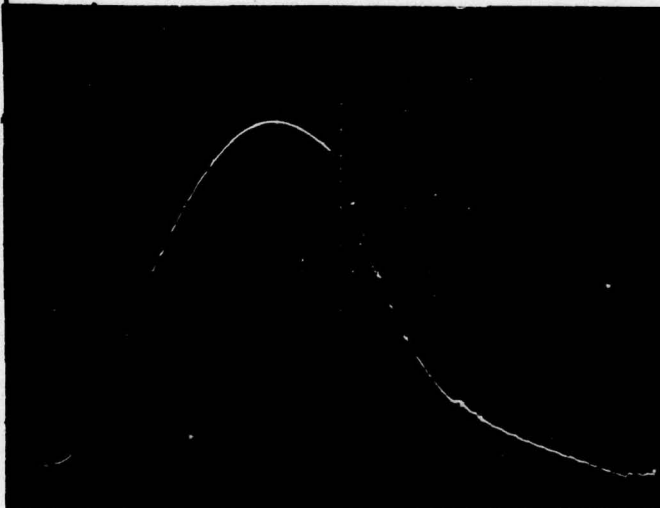


(L<sub>q</sub>)

50 A / DIV.

5  $\mu$  SEC / DIV.

11 KW, 0.8 PF LOAD



SHORT CIRCUIT  
3 $\phi$ , L-T-N

DISTRIBUTION:

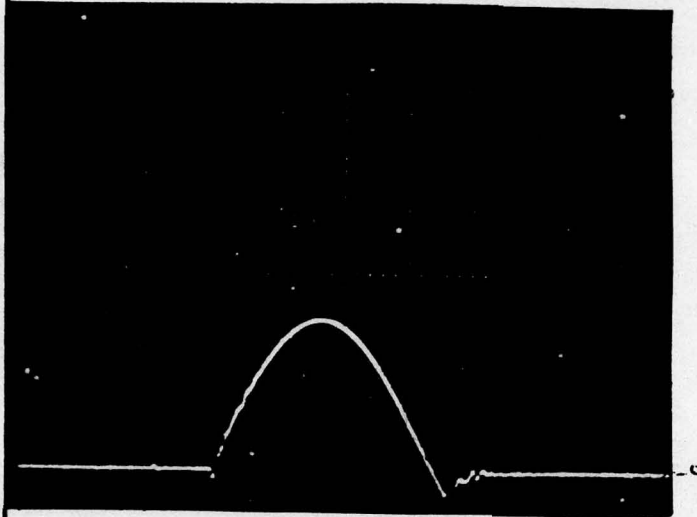
TITLE

PREPARED CORRY 5/5/75 DATE

CHECKED

APPROVED

THYRISTOR CURRENTS 60 HZ

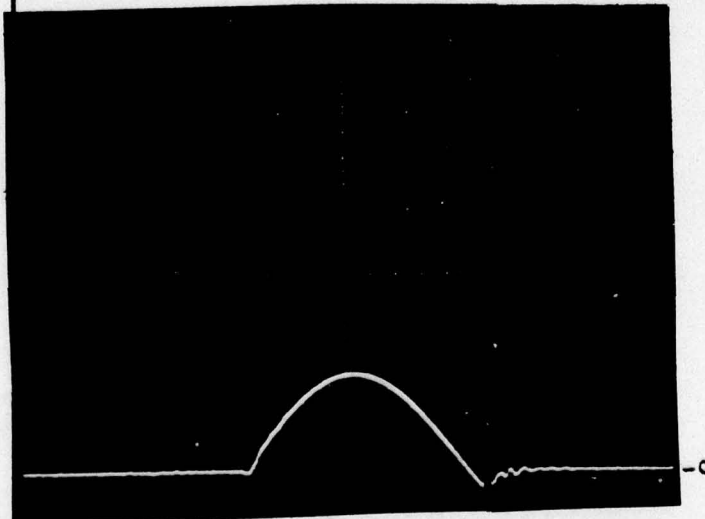


$T_c^+$

50A / DIV.

5  $\mu$  SEC / DIV.

11KV, 0.8PF LOAD



SHORT CIRCUIT  
3 $\phi$ , L-T-N

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GENERAL MOTORS CORPORATION

REPORT NO.

ITEM NO.

0009

PAGE

JOB NO.

DESIGN

DATA

PAGE

26

TITLE

PREPARED

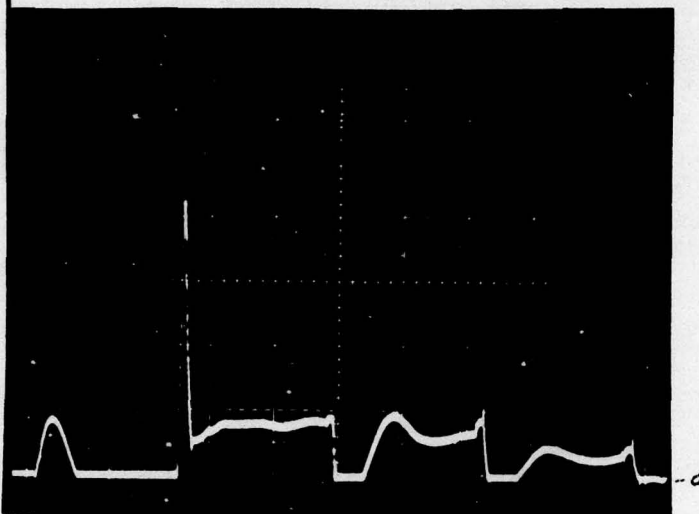
CORY

DATE

5/5/75

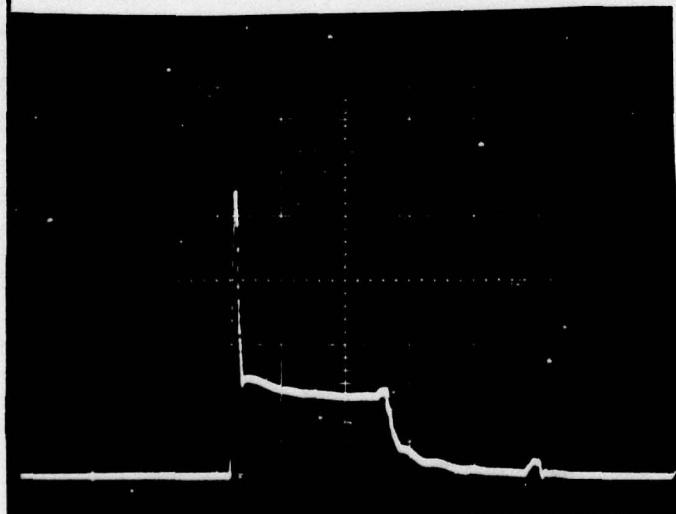
CHECKED

APPROVED

THYRISTOR CURRENTS 60 HZ

(T+)

50A / DIV.

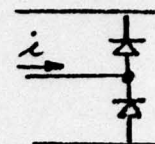
200  $\mu$  SEC / DIV.11 KW, 0.8 PF LOADSHORT CIRCUIT30 L-T-N

DISTRIBUTION:

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	TITLE		PREPARED CORRY	DATE 5/5/75
		CHECKED		
		APPROVED		

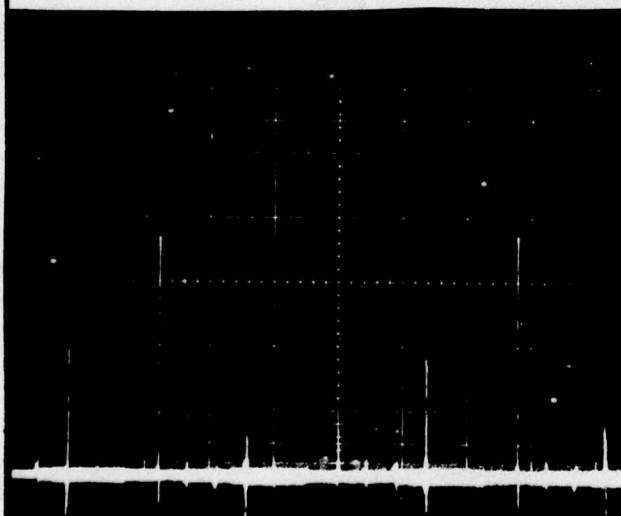
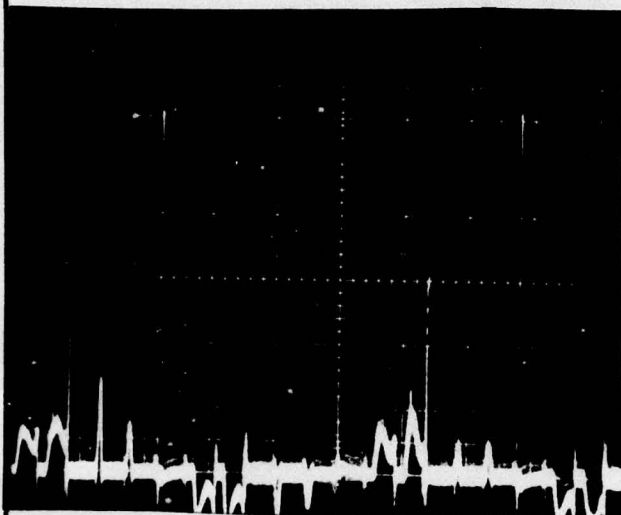
# DIODE CURRENTS 60 HZ

T<sup>+</sup> BY-PASS DIODES



20 A / DIV.  
1 ms / DIV.

11 KW, 0.8 PF LOAD



SHORT CIRCUIT  
3Φ, L-T-N

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GENERAL MOTORS CORPORATION

REPORT NO.

ITEM NO.  
0009

PAGE

JOB NO.

DESIGN  
DATA

PAGE

28

TITLE

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CORRY 5/5/75

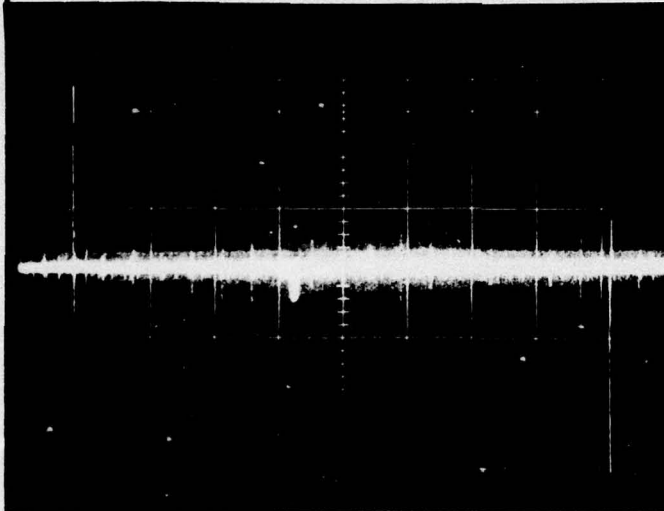
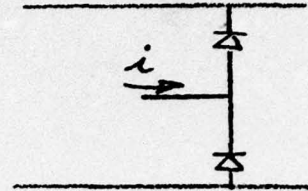
DATE

CHECKED

APPROVED

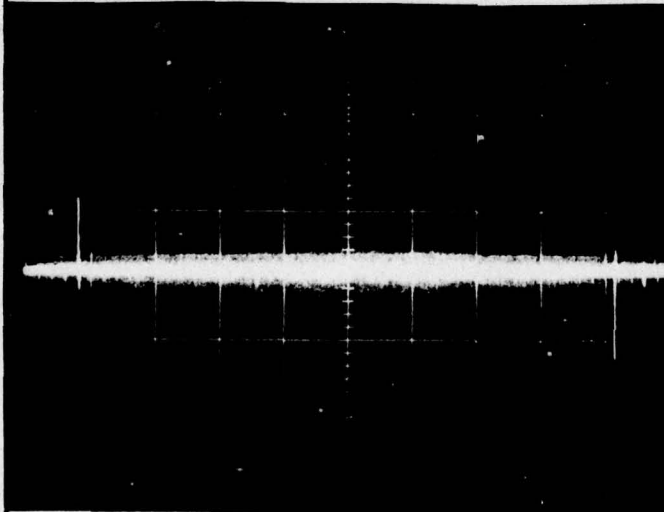
DIODE CURRENTS 60 HZ

POWER CENTER  
BY-PASS DIODES



50A/DIV.  
1MS/DIV.

11KW, 0.8 PF LOAD



100A/DIV.  
1MS/DIV.

SHORT CIRCUIT  
3Q, L-T-N

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GENERAL MOTORS CORPORATION

REPORT NO.

ITEM NO.  
0009

PAGE

JOB NO.

DESIGN  
DATA

PAGE

29

TITLE

PREPARED

CORRY

DATE

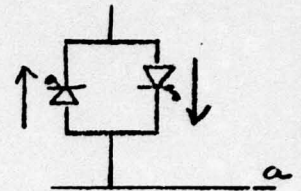
5/5/75

CHECKED

APPROVED

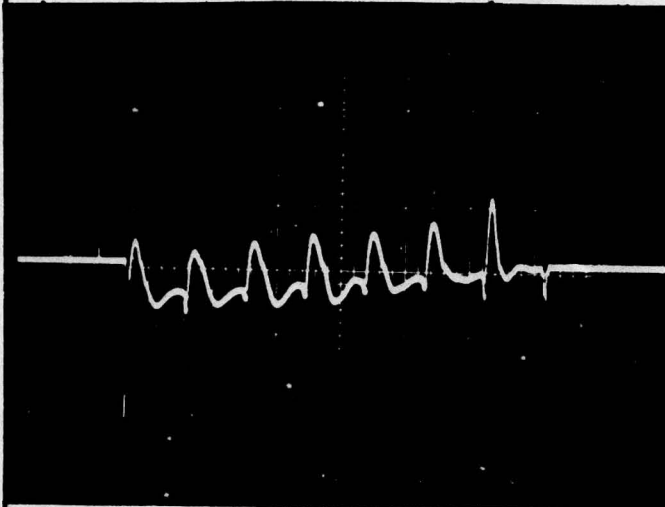
THYRISTOR CURRENTS 60Hz

$R_C$

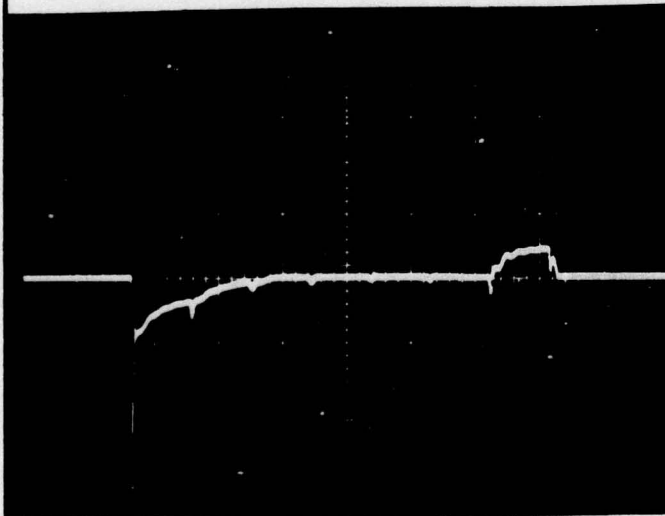


100A/DIV.  
0.5MS/DIV.

11KW, 0.8 PF LOAD



PC 3 | 2 | 1 | 0 | 1 | 2 | 3 |



PC 3 | 2 | 1 | 0 | 1 | 2 | 3 |

SHORT CIRCUIT  
3 $\phi$ , L-T-N

( $R_C$  TURNS OFF BY  
STARVATION AT END  
OF 3/2 STEP, SEE  
PAGE 38)

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GENERAL MOTORS CORPORATION

REPORT NO.

ITEM NO.  
0009

PAGE

JOB NO.

DESIGN  
DATA

PAGE

30

TITLE

PREPARED

CORRY

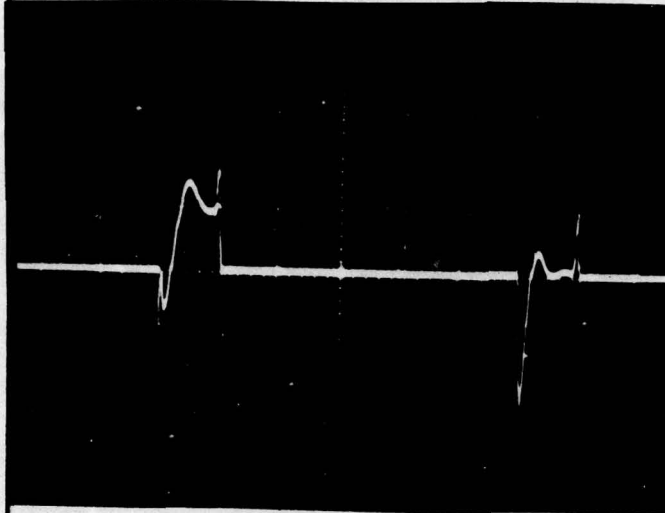
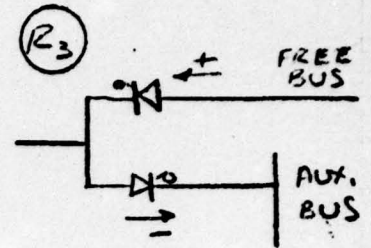
DATE

5/5/75

CHECKED

APPROVED

THYRISTOR CURRENTS 60 HZ

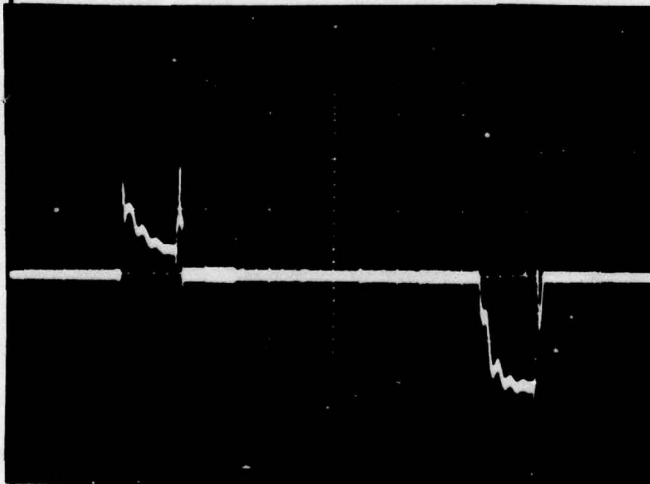


↑ +  
0  
↓ -

50 A/DIV.

500 μSEC/DIV.

11KW, 0.8PF LOAD



↑ +  
0  
↓ -

SHORT CIRCUIT  
3Φ, L-T-N

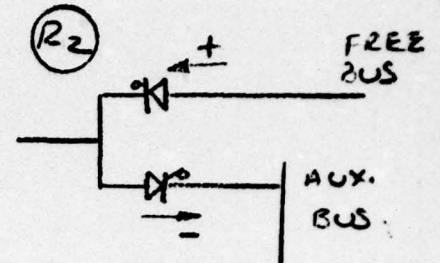
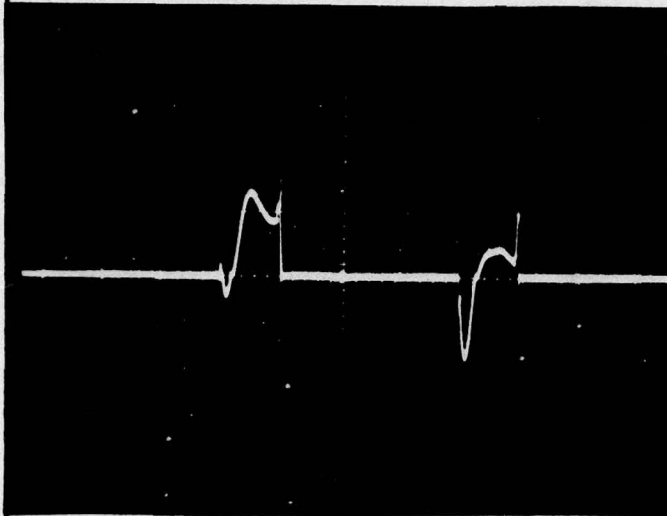
20 A/DIV.

DISTRIBUTION:

TITLE

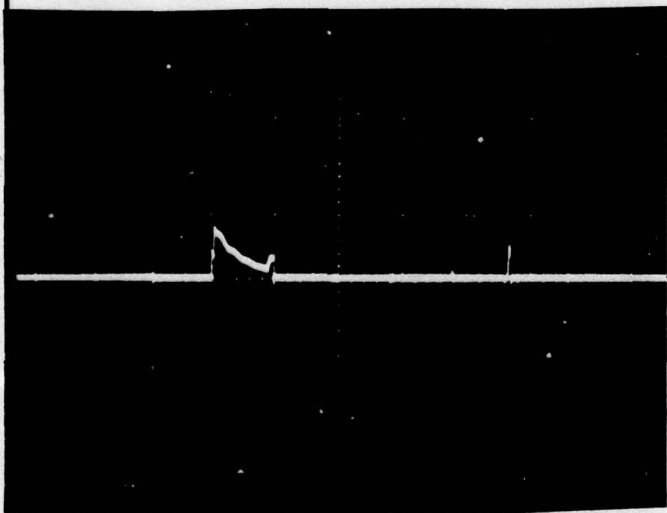
PREPARED CORRY DATE 5/5/75  
CHECKED  
APPROVED

THYRISTOR CURRENTS 60Hz



50 A / DIV.  
500  $\mu$  SEC / DIV.

11 KW, 0.8 PF LOAD



SHORT CIRCUIT  
3 $\phi$ , L-T-N

DISTRIBUTION:

TITLE

PREPARED

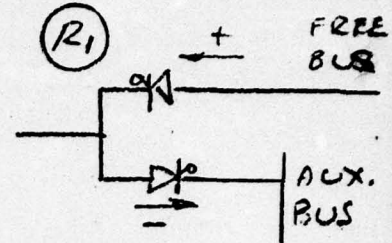
DATE

CORRY 5/5/75

CHECKED

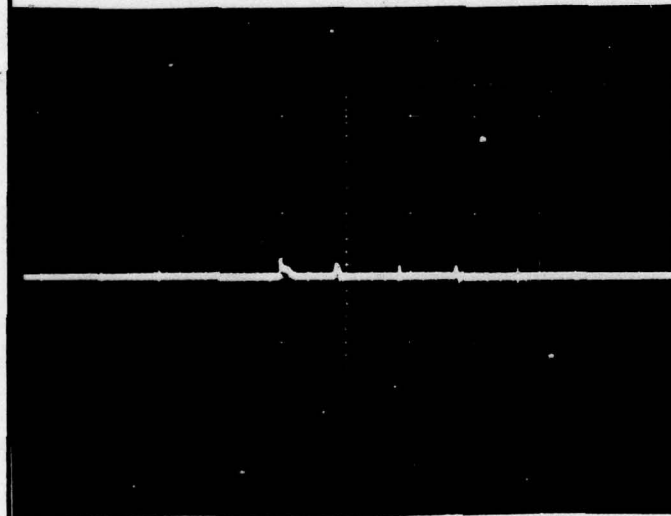
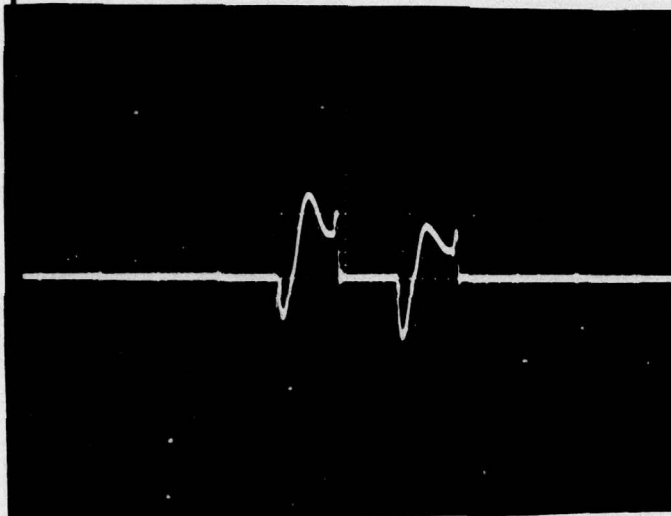
APPROVED

THYRISTOR CURRENTS 60 HZ



50A/DIV.  
500 μSEC/DIV.

11 KW, 0.8 PF LOAD



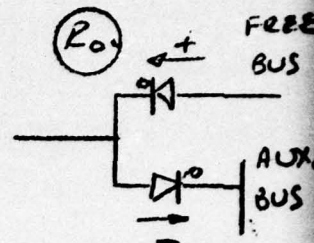
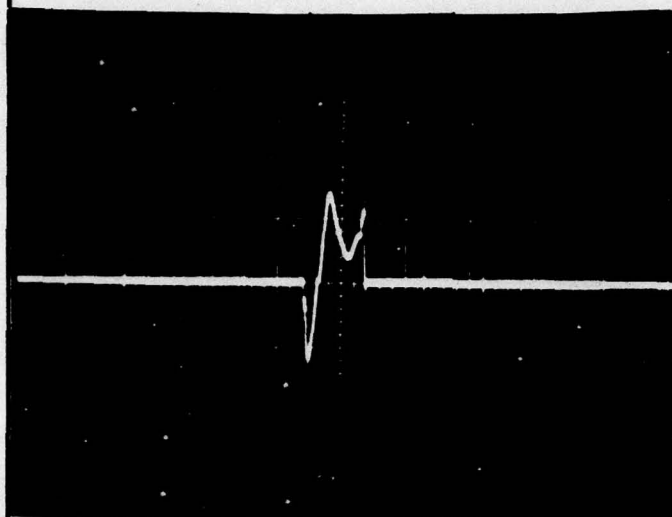
SHORT CIRCUIT  
3φ, L-T-N

DISTRIBUTION:

TITLE

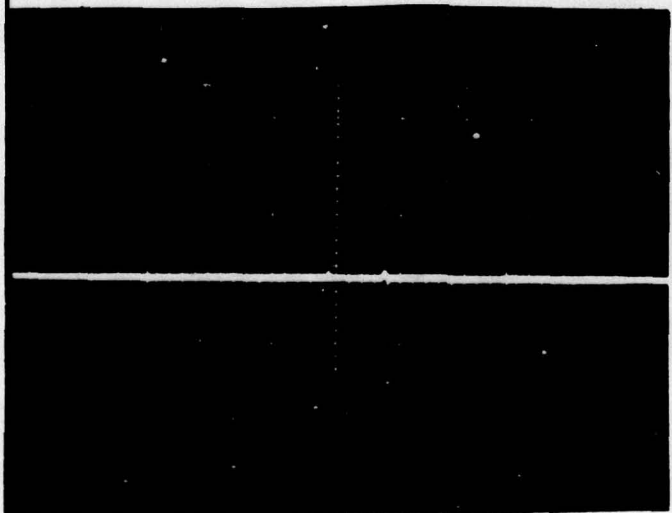
PREPARED  
CORRY  
DATE  
5/5/75  
CHECKED  
APPROVED

THYRISTOR CURRENTS 60 HZ



50 A / DIV.  
500  $\mu$  SEC / DIV.

11KW, 0.8 PF LOAD

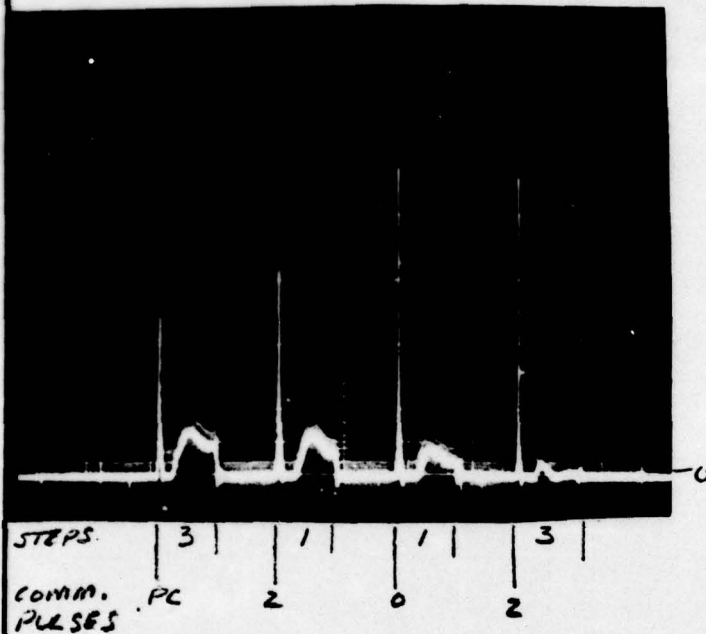


SHORT CIRCUIT  
3 $\phi$ , L-T-N

DISTRIBUTION:

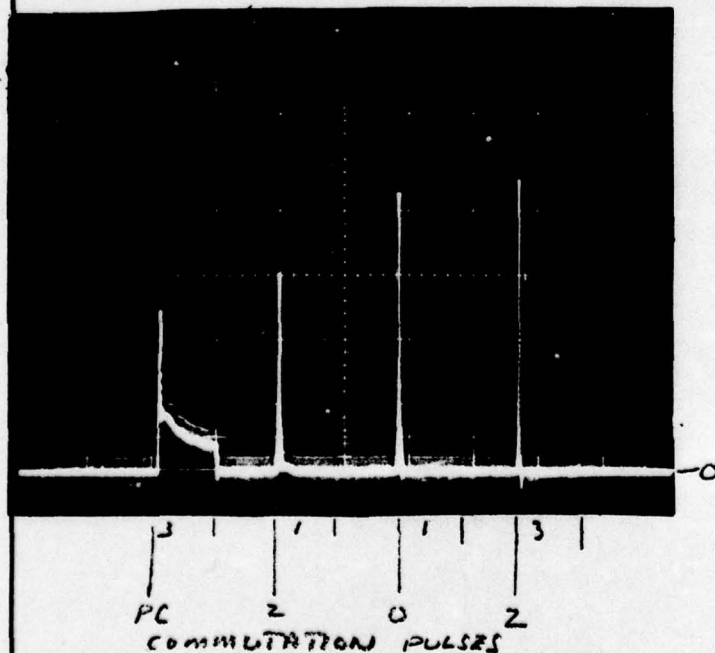
DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0009	PAGE	JOB NO. DESIGN DATA	PAGE 34
	TITLE THYRISTOR CURRENTS 60 HZ		PREPARED CORY 5/5/75	DATE 5/5/75
		CHECKED		
		APPROVED		

(RSA)



100A/DIV.  
500μSEC/DIV.

11KW, 0.8PF LOAD



SHORT CIRCUIT  
3φ, L-T-N

DISTRIBUTION:

TITLE

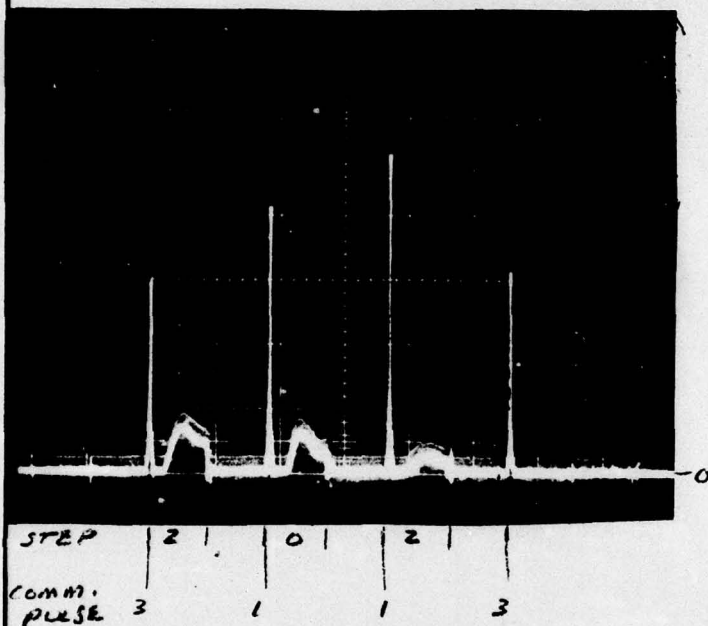
PREPARED CORR-1 DATE 5/5/75  
CHECKED  
APPROVED

THYRISTOR CURRENTS 60 HZ

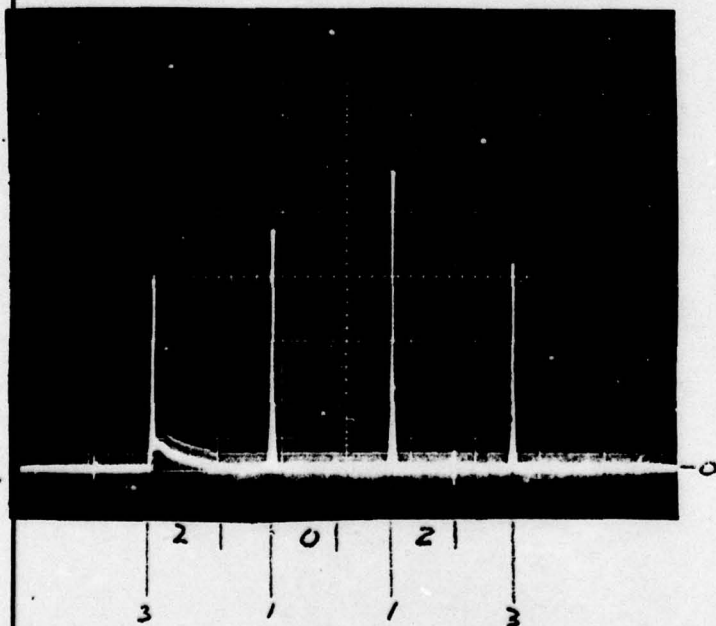
(RSB)

100 A / DIV.  
500  $\mu$  SEC / DIV.

11KW, 0.8 PF LOAD



SHORT CIRCUIT  
3 $\phi$ , L-T-N

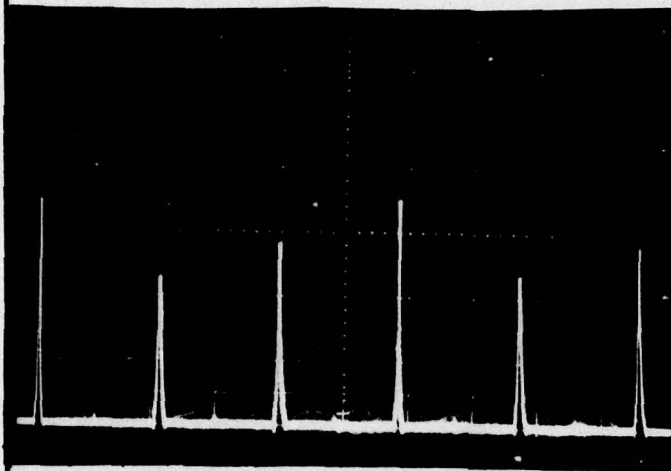


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DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0009	PAGE	JOB NO. DESIGN DATA	PAGE 36
	TITLE		PREPARED CORRY 5/5/75	DATE
		CHECKED		
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THYRISTOR CURRENTS 60 HZ

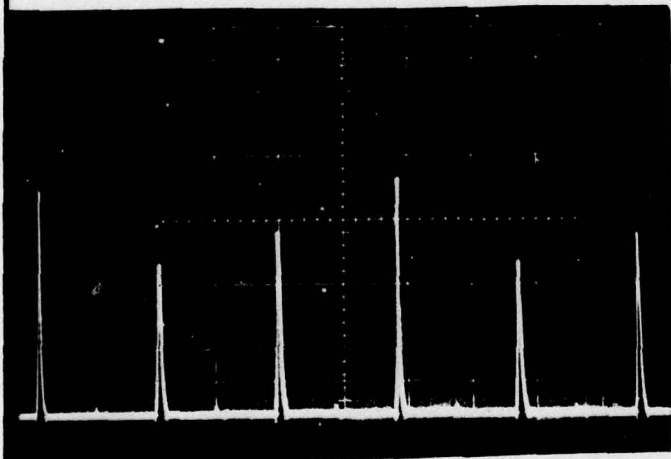
(A)



100 A / DIV.  
500  $\mu$  SEC / DIV.

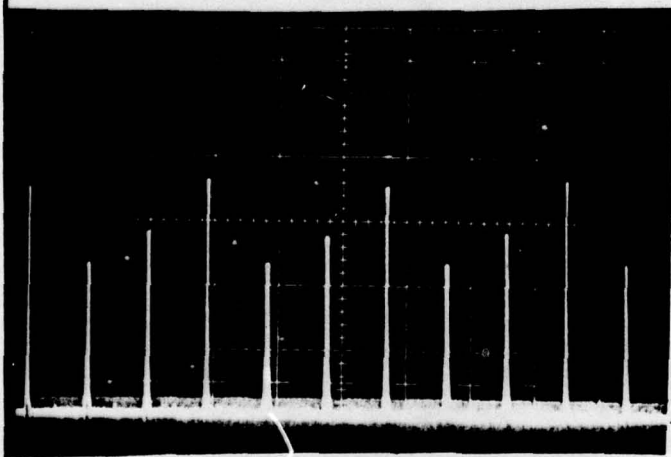
11 KW, 0.8 PF LOAD

( $V_B = 66 \text{ VDC}$ ;  $I_B = 2 \text{ A}$ )



SHORT CIRCUIT  
3 $\phi$ , L-T-N

500  $\mu$  SEC / DIV.



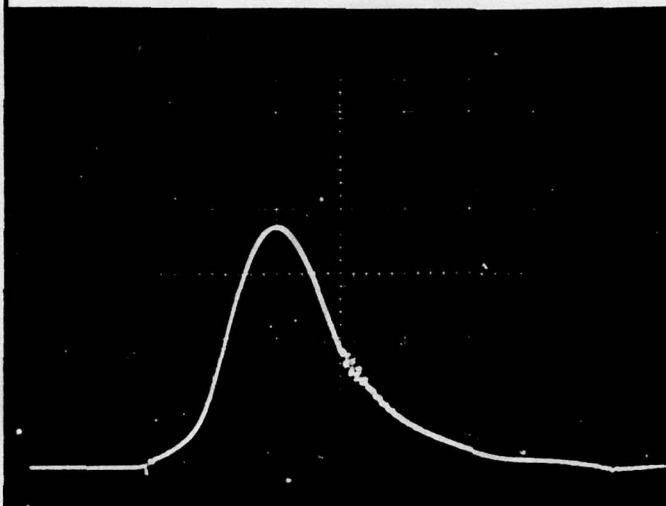
1 MS / DIV.

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DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0009	PAGE	JOB NO. DESIGN DATA	PAGE 37
	TITLE		PREPARED CORRY 5/5/75	DATE
		CHECKED		
		APPROVED		

TH-11215702 CURRENTS 60HZ

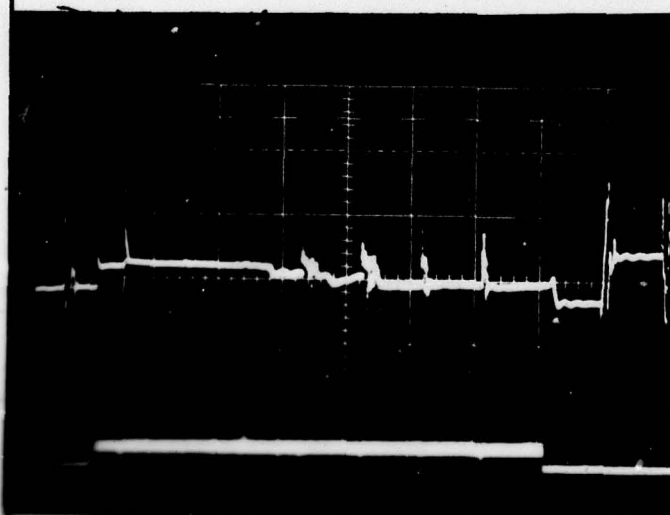
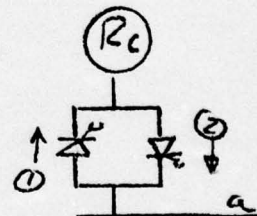
(A)



100A/DIV.  
10μsec/DIV.

(SAME CONDITIONS AS  
PAGE 37)

TURN OFF OF  $I_{C_1}$ . (SEE PAGE 30)  
SHORT CIRCUIT CONDITIONS.



↑ 10V/DIV.  
500μsec/DIV

① REVERSE BIASED BY  $P\bar{C}$

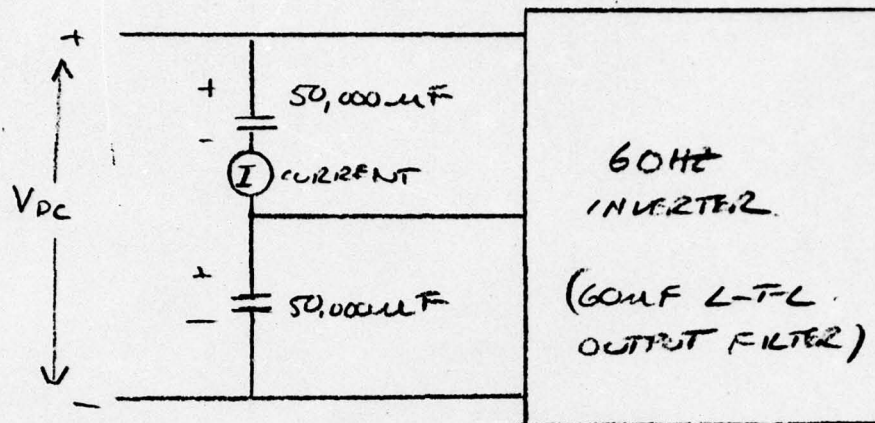
② RINGS UP WHEN  $P\bar{C}$   
TURNS ON AFTER  $R_3$

GATE  
TRIGGER

DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0009	PAGE	JOB NO. DESIGN DATA	PAGE 38
	TITLE		PREPARED CORY 5/5/75	DATE
		CHECKED		
		APPROVED		

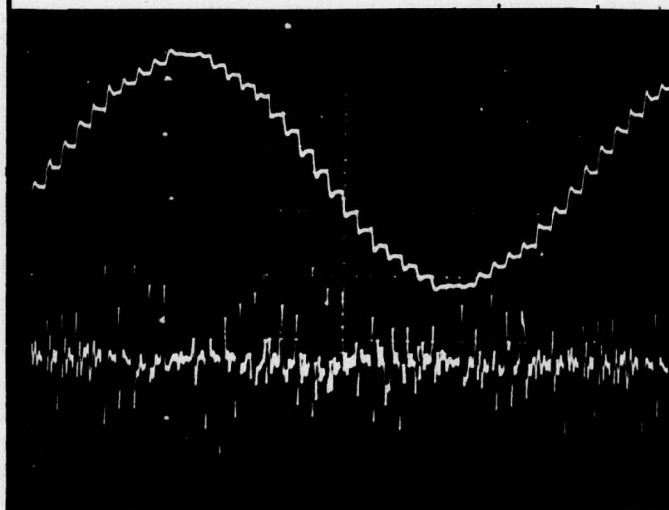
# INVERTER INPUT FILTER CAPACITOR CURRENT 60 HZ

CONV.  
CKT.



$$V_B = 66 \text{ VDC}$$

$$I_B = 8 \text{ ADC}$$



INVERTER OUTPUT VOLTAGE



FILTER CAPACITOR CURRENT

50 A/DIV. 2 MS/DIV.

NO LOAD

SAME AS ABOVE

17.5 A RMS MEASURED  
ON A.P. TRUE  
RMS METER

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GENERAL MOTORS CORPORATION

REPORT NO.

ITEM NO.

0009

PAGE

JOB NO.

DESIGN

DATA

PAGE

39

TITLE

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CORRY 5/5/75

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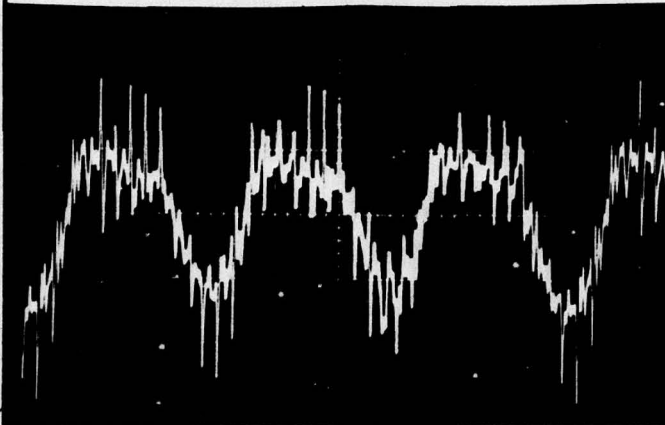
APPROVED

INVERTER INPUT FILTER CAPACITOR CURRENT

60HZ

CONV.

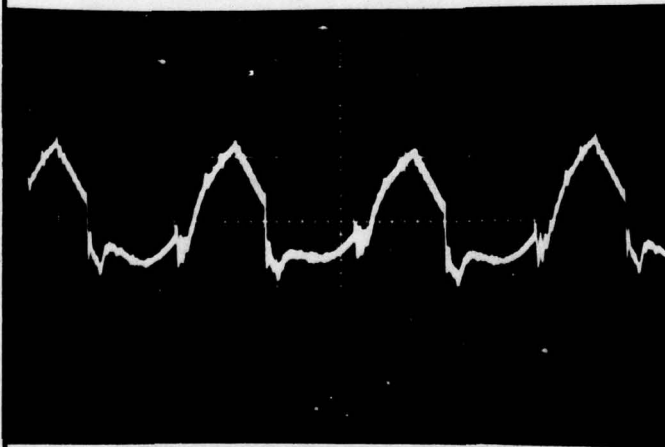
CKT.

FILTER CAPACITOR CURRENT

50A/DIV. 2ms/DIV.

11KW, 0.8PF LOAD50A. RMS

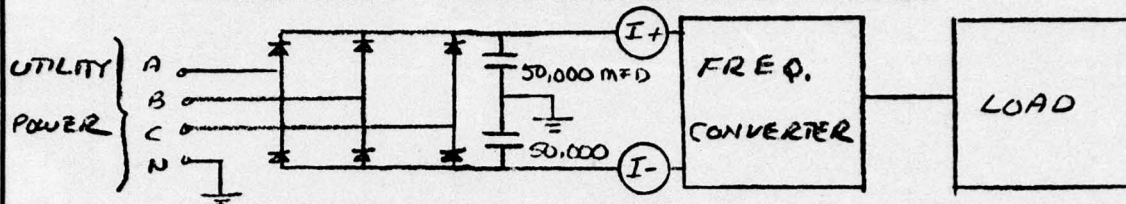
(TRIPLER FREQUENCY 180HZ)

SHORT CIRCUIT3Φ, L-T-N32A. 12MS

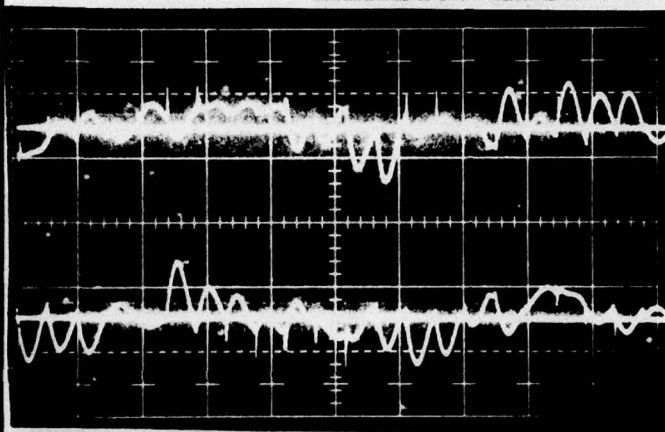
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<b>DELCO ELECTRONICS</b> GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO.	PAGE JOB NO.	DESIGN DATA	PAGE 39A
	TITLE		PREPARED CORRY	DATE 5/5/76
		CHECKED		
		APPROVED		

### CIRCUIT DESIGN TEST DATA 60HZ



### INVERTER INPUT CURRENT - 60HZ 3 PHASE

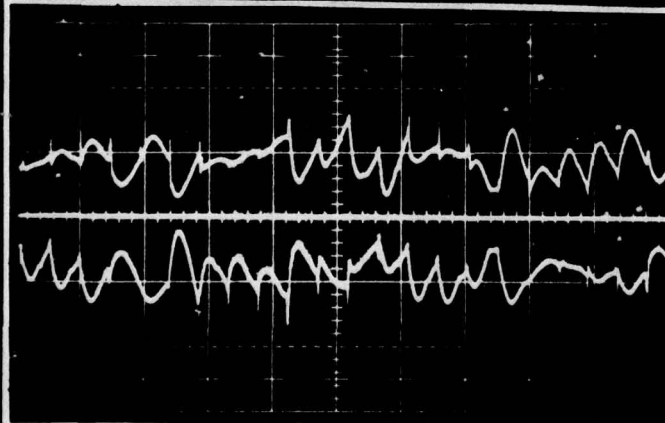


I+

NO LOAD INPUT  
CURRENT

50A/DIV.  
1ms/DIV

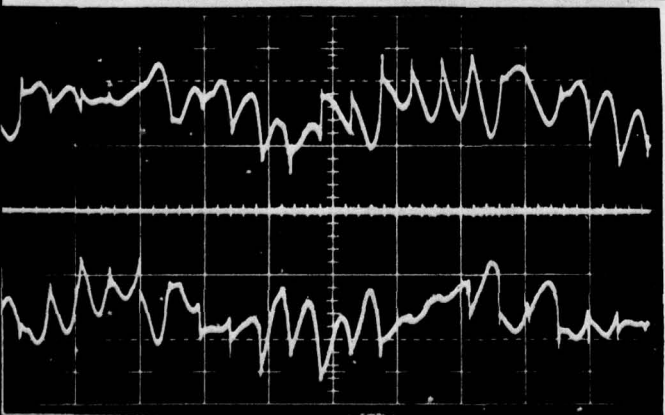
I-



I+

11KW, PF=0.8

I-



I+

20.6 KW, PF=0.8

I-

DISTRIBUTION:

TITLE

PREPARED

CORRY

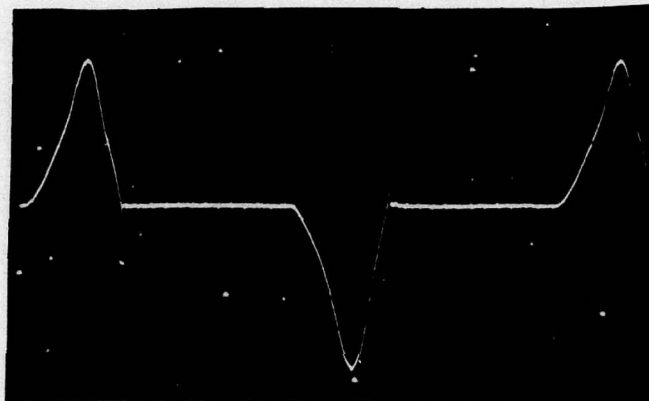
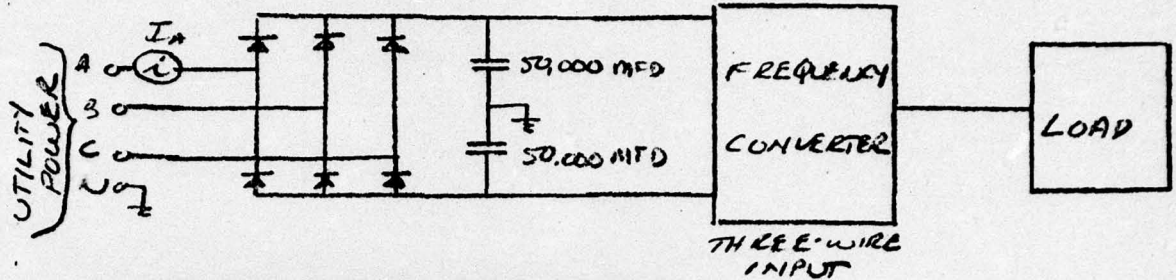
DATE

5/5/78

CHECKED

APPROVED

CURRENT WAVEFORMS-POWER LINES  
AT INPUT TO RECTIFIER

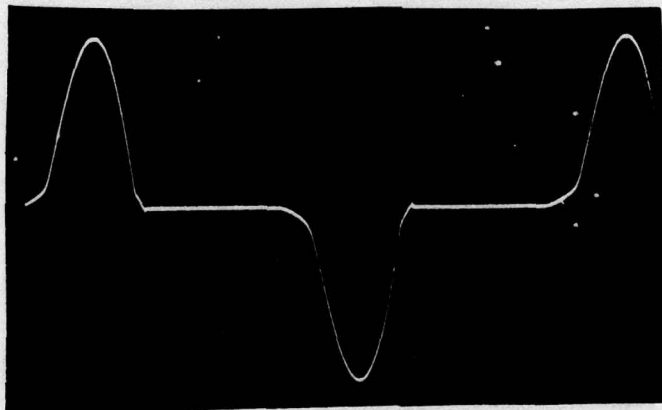


60 HZ UTILITY LINE  
CURRENTS  $I_a$

NO LOAD ON  
FREQUENCY CONVERTER

↑ 10A/DIV. ↔ 2MS/DIV.

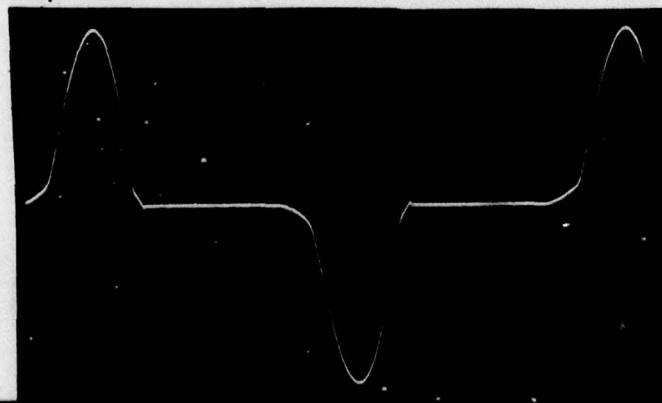
8.38 AMPS RMS



11KW, PF=1.0, 400 HZ  
3Φ LOAD ON F.C.

↑ 50A/DIV. ↔ 2MS/DIV.

56.6 AMPS RMS



11KW, PF=0.8

↑ 50A/DIV. ↔ 2MS/DIV.

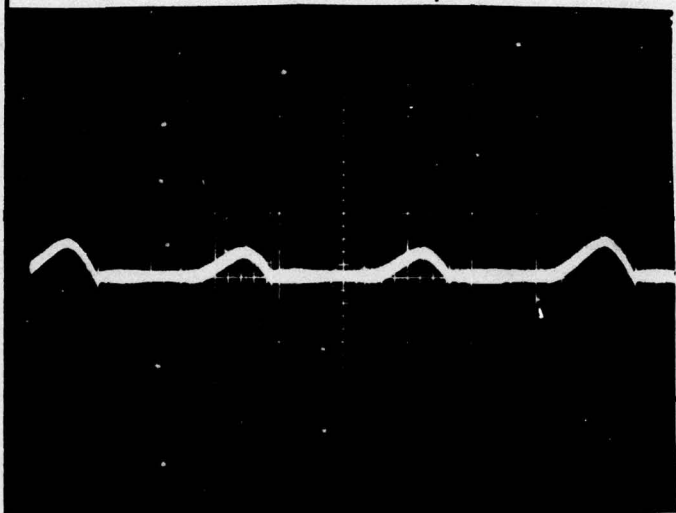
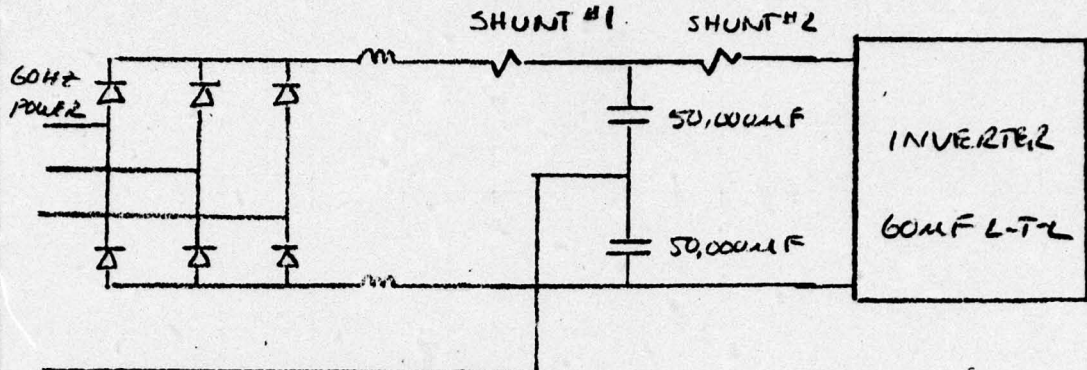
56 AMPS RMS

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	TITLE		PREPARED CORRY 5/5/75	DATE
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RECTIFIER CURRENTS INTO INPUT FILTER

60Hz CONV. CRT.

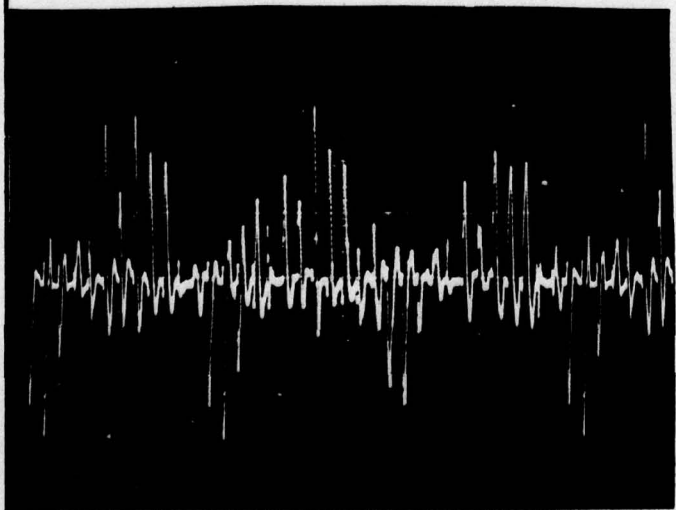


SHUNT #1

20A/DIV.

2ms/DIV

NO LOAD



SHUNT #2

20A/DIV.

2ms/DIV

NO LOAD

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REPORT NO.

ITEM NO.

0009

PAGE

JOB NO.

DESIGN

DATA

PAGE

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TITLE

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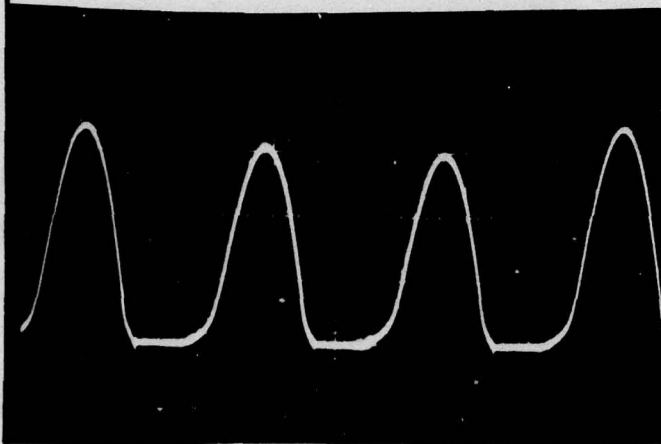
CORRY

DATE

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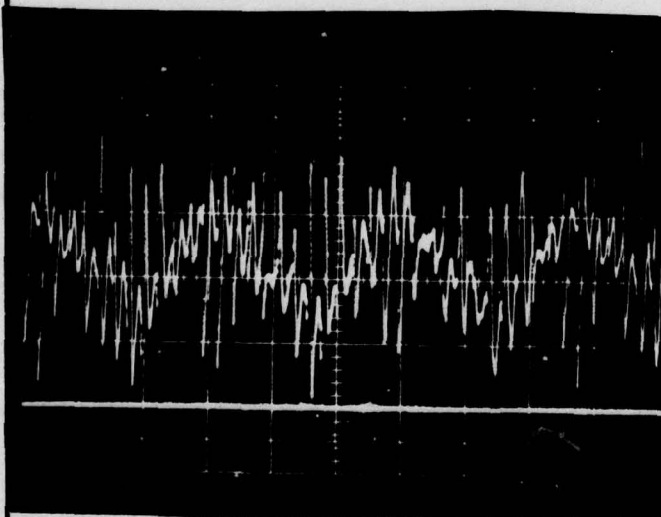
SHUNT #1

40 A/DIV.

2 MS/DIV.

11KW, 0.8PF LOAD

(120A PEAK CURRENTS)



SHUNT #2

20 A/DIV.

2 MS/DIV.

11KW, 0.8 PF LOAD

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REPORT NO.  
ITEM NO.  
0009

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DESIGN  
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PAGE

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TITLE

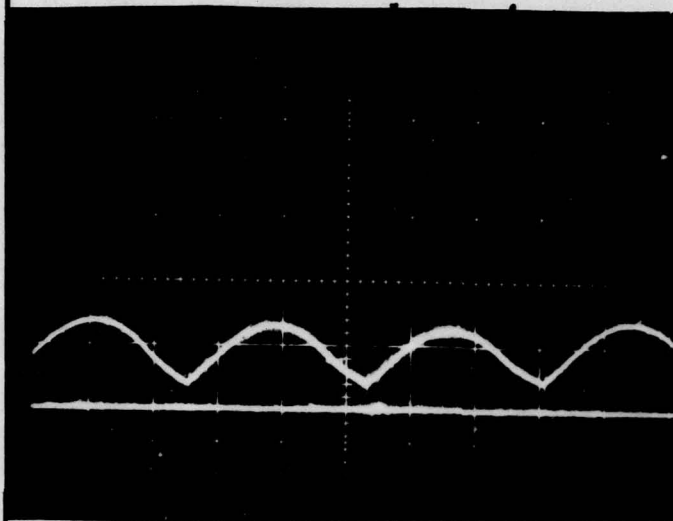
PREPARED

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SHUNT #1

100A/DIV

2ms/DIV

SHORT CIRCUIT

3 $\phi$ , L-T-N

0 (140 A PEAK)



SHUNT #2

100A/DIV

2ms/DIV

SHORT CIRCUIT

3 $\phi$ , L-T-N

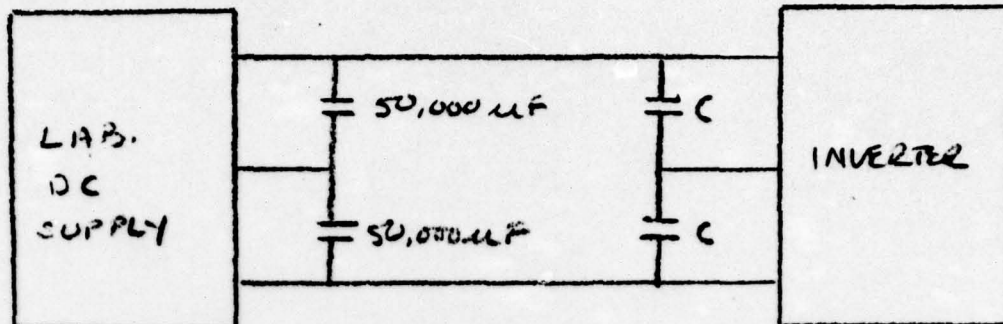
0

DISTRIBUTION:

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	TITLE		PREPARED CORRY 5/5/75	DATE
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# INPUT FILTER EXPERIMENT

60Hz CONV. CKT



DETERMINATION OF VALUE OF C REQUIRED TO PERMIT TWO WIRE INPUT TO INVERTER FOR 60Hz OPERATION.

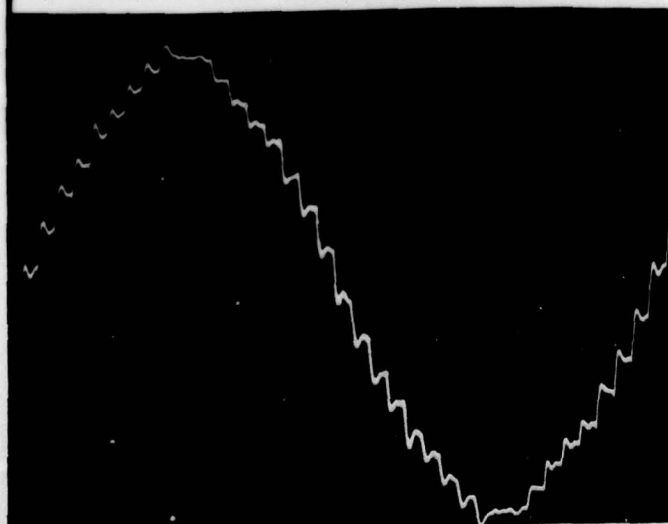


OUTPUT VOLTAGE

$$C = 375 \text{ MFD}$$

4.4 KW, 0.8 PF LOAD, 3P

$$\text{THD} = 5.5\%$$



11 KW, 0.8 PF LOAD, 3P

$$\text{THD} = 5.8\%$$

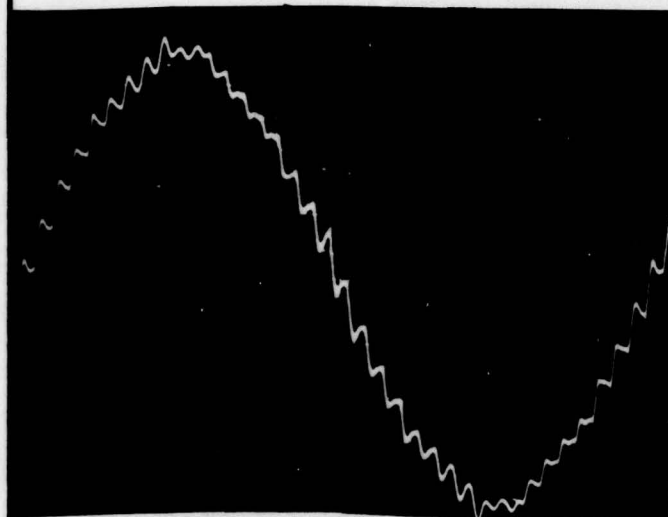
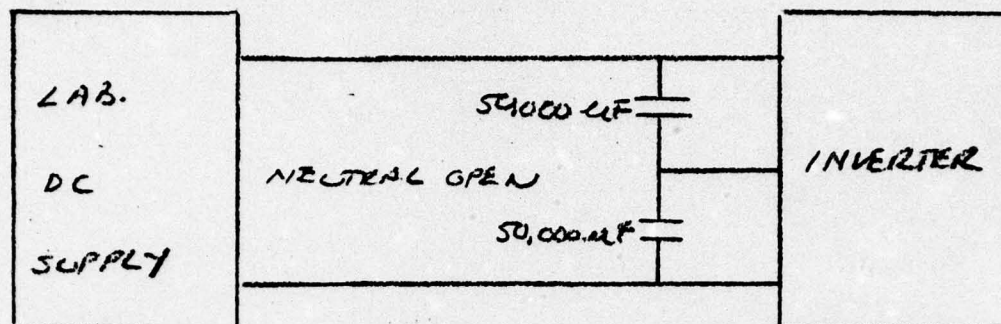
(INVERTER WORKS WELL WITH 3P BALANCED LOADS AND LOW INPUT CAPACITANCE. CAN NOT SUPPLY UNBALANCED LOADS.)

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	TITLE		PREPARED CORRY 5/5/71	DATE
		CHECKED		
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# INPUT FILTER EXPERIMENT

60Hz CONV. CKT



## OUTPUT VOLTAGE

4 KVA 1 $\phi$  LOAD  
CONNECTED BE-  
TWEEN PHASES  
A AND B.

THD = 5.7%

DISTRIBUTION:

TITLE

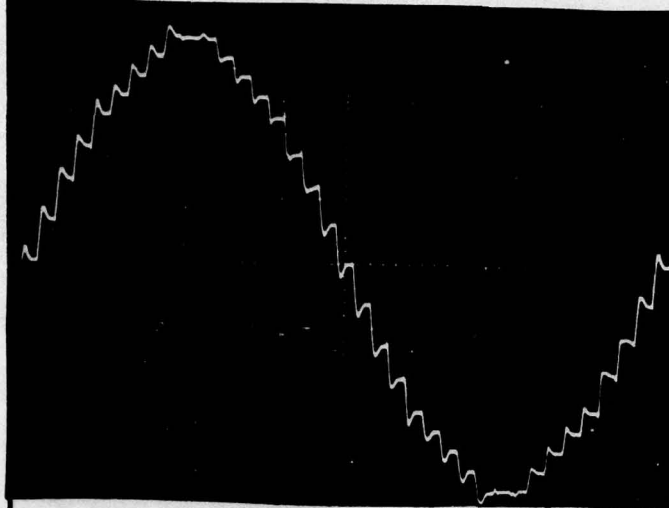
PREPARED CORRY 5/5/75 DATE

CHECKED

APPROVED

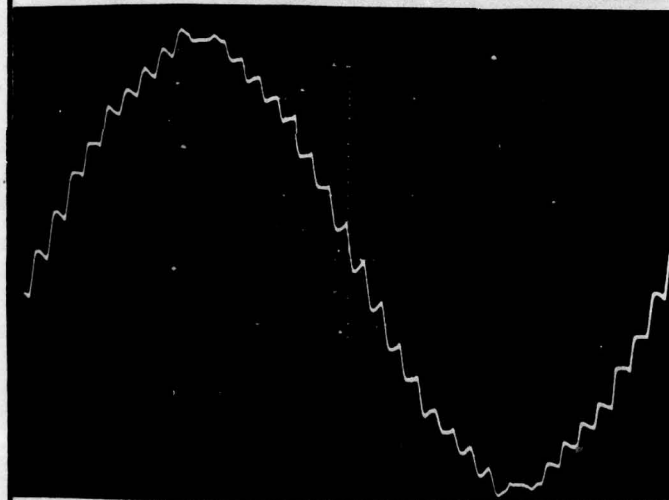
STUDY OF THD AS A FUNCTION OF OUTPUT  
FILTER L-T-L CAPACITANCE. 60HZ, CONV. CRT.

NO LOAD TESTS



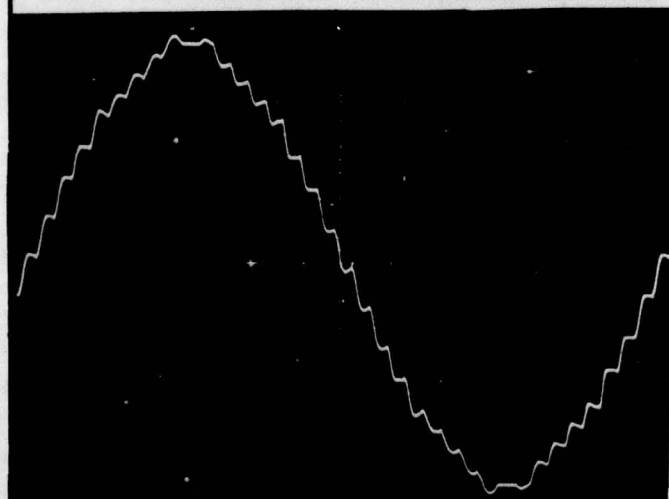
60 MFD. L-T-L

THD = 5.9%



120 MFD. L-T-L

THD = 4.85%



180 MFD. L-T-L

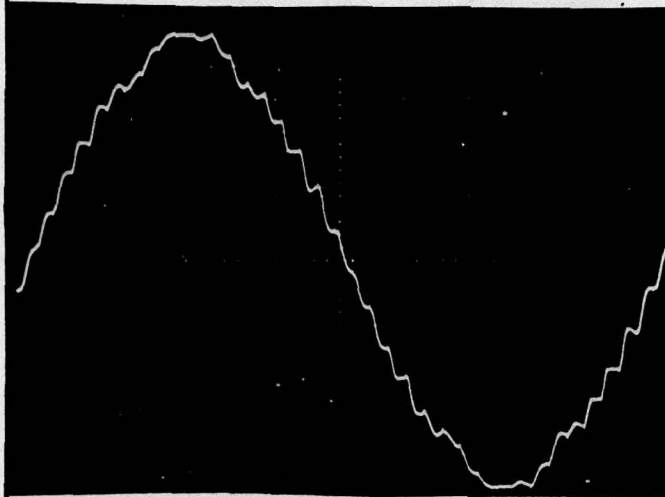
THD = 4.15%

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APPROVED

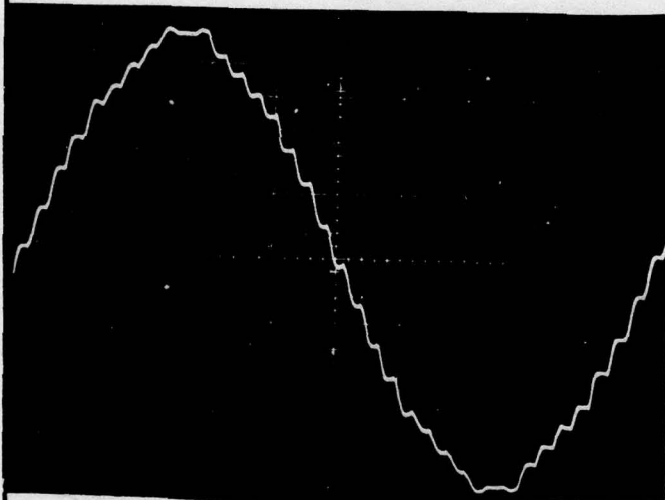
THD. VS OUTPUT CAPACITANCE



180 MFD. L-T-L

(WITH 100μH ADDED  
IN SERIES WITH  
EACH DC INPUT LINE)

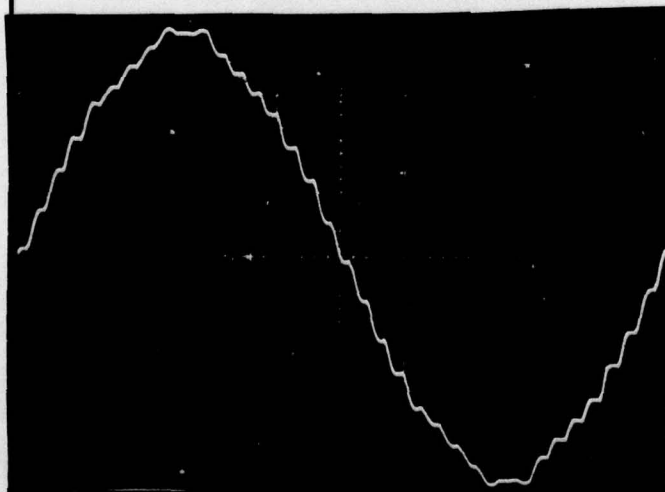
THD = 4.17%



240 MFD. L-T-L

THD = 3.7%

(THD = 3.6% WITH  
11KW, 0.8 PF LOAD).



290 MFD. L-T-L

THD = 3.45%

DISTRIBUTION:

TITLE

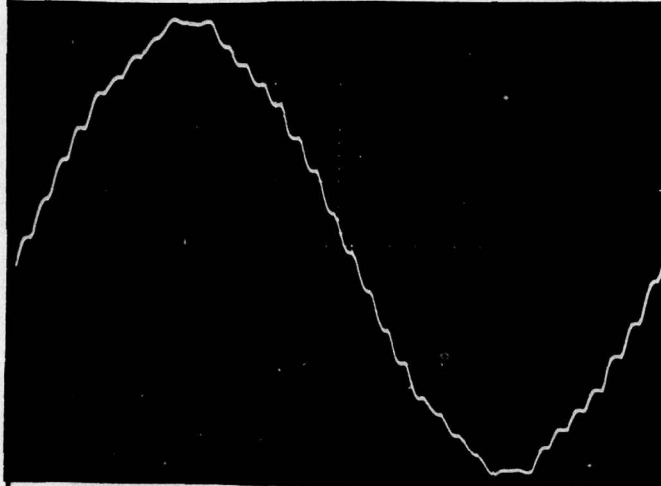
PREPARED

DATE

CHECKED

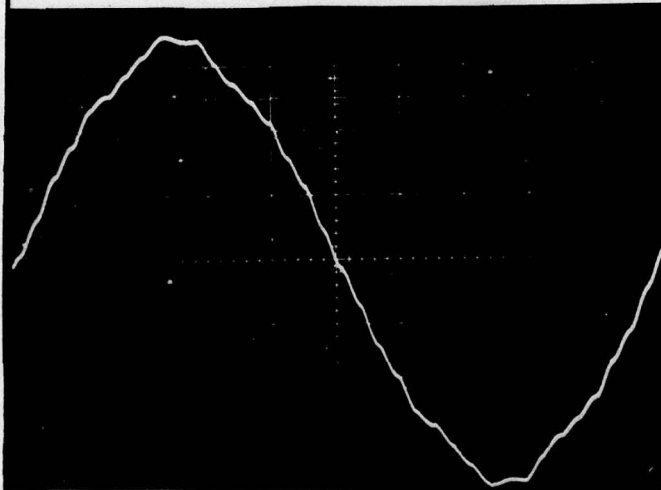
APPROVED

THD. VS OUTPUT CAPACITANCE



340 MFD. L-T-L

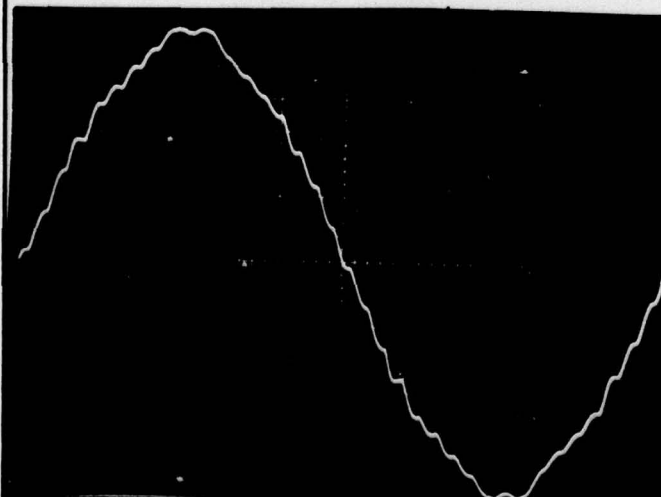
THD = 3.3%



340 MFD L-T-L

(EXTRA TRIPLIN  
ADDED)

THD = 2.9%



340 MFD L-T-L PLUS  
250 MFD L-T-N

• THD = 3.2%

DISTRIBUTION:

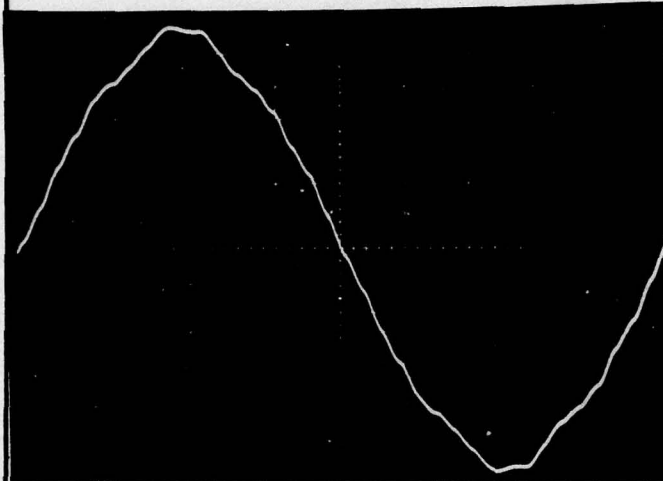
TITLE

PREPARED CORRY 5/5/75

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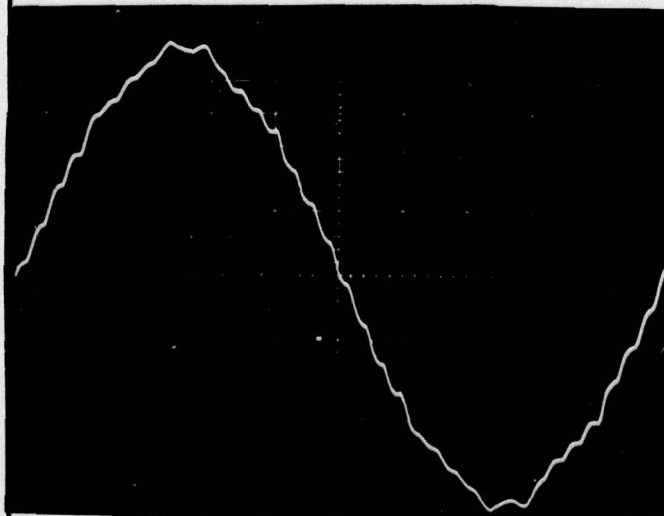
THD. VS OUTPUT CAPACITANCE



340 MFD L-T-L PLUS  
250 MFD L-T-N

(EXTRA TRIPLEN  
ADDED)

THD = 2.83%



340 MFD L-T-L PLUS  
250 MFD L-T-N

11KW, 0.8 PF LOAD

THD = 3.0%

DISTRIBUTION:

AD-A035 046

GENERAL MOTORS CORP GOLETA CALIF DELCO ELECTRONICS DIV  
GENERATOR SET, 100KW FREQUENCY CONVERTER.(U)  
JUL 75 T CORRY

F/6 9/5

UNCLASSIFIED

R75-64

DAAK02-72-C-0210

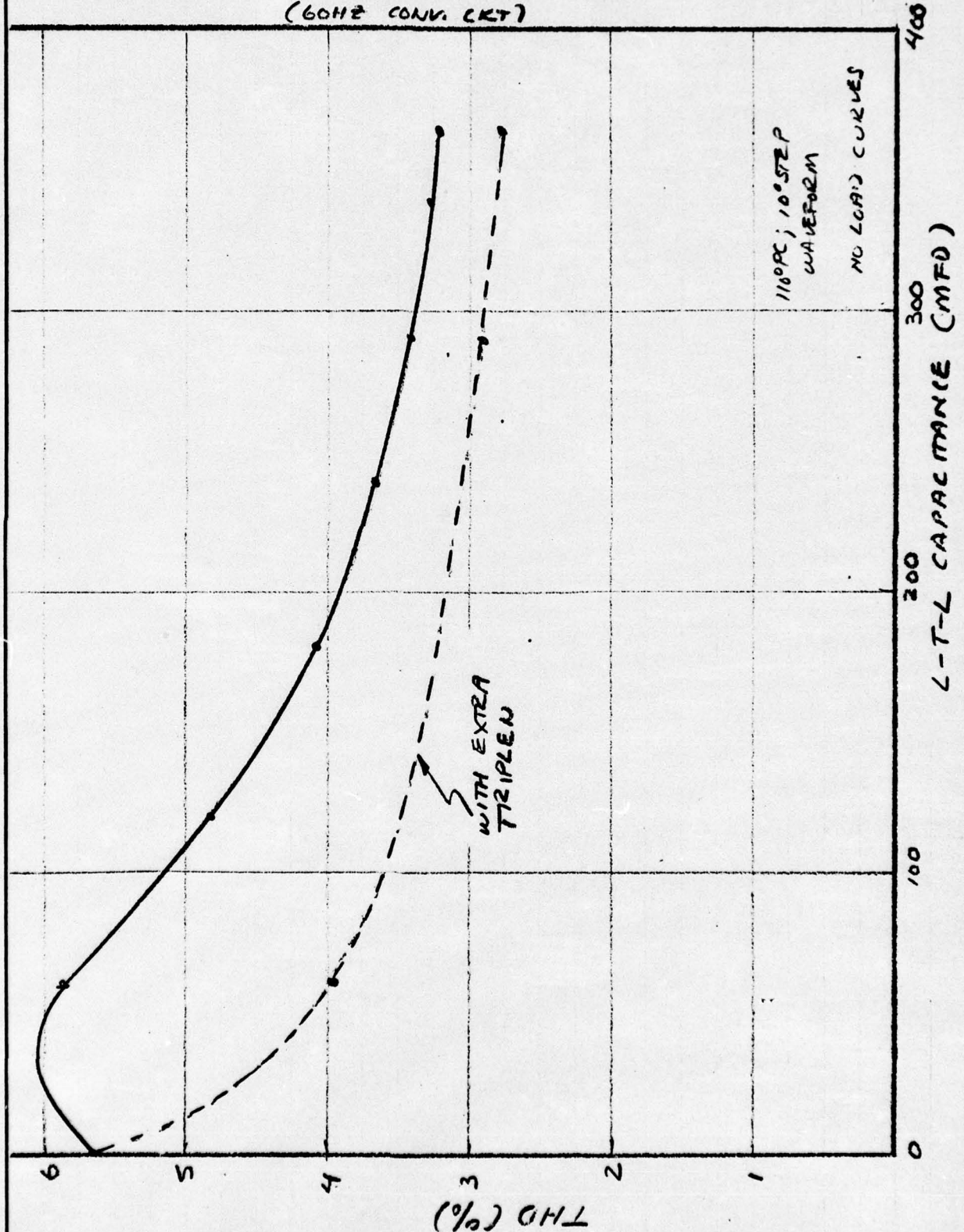
NL

2 OF 2  
AD  
A035046



DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0009	PAGE	JOB NO. DESIGN DATA	PAGE 49
	TITLE		PREPARED CORY	DATE 5/5/75
		CHECKED		
		APPROVED		

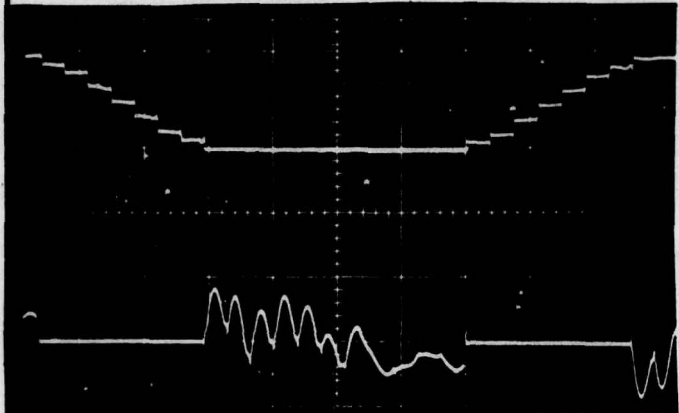
PLOTS OF THD OF INVERTER OUTPUT VOLTAGES VS L-T-L FILTER CAPACITANCE  
(60HZ CONV. CRT)



DISTRIBUTION:

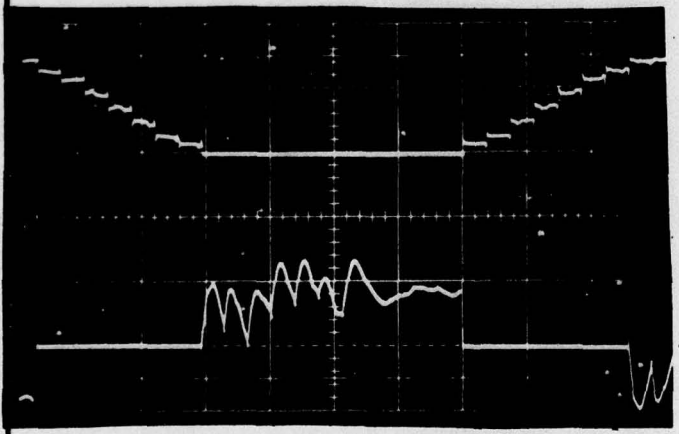
DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0009	PAGE JOB NO. DESIGN DATA	PAGE 50
	PREPARED CORRY		DATE
TITLE POWER CENTER THYRISTOR VOLTAGES AND CURRENTS 60HZ, THREE PHASE		CHECKED	
		APPROVED	

POWER CENTER THYRISTOR VOLTAGES AND CURRENTS  
60HZ, THREE PHASE

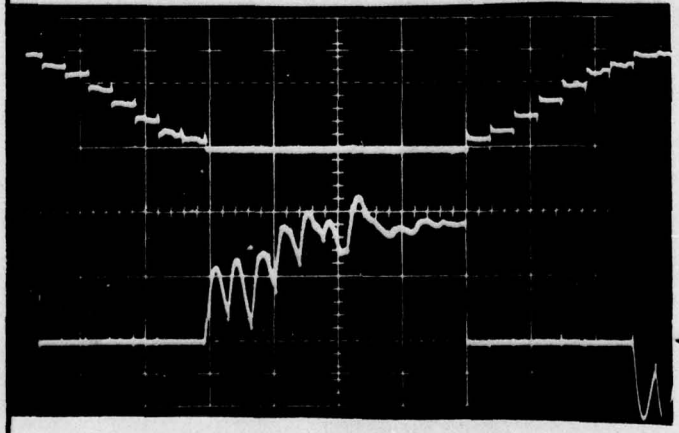


POWER CENTER  
 THYRISTOR VOLTAGE  
 200 V/DIV.  
 NO LOAD

THYRISTOR & DIODE CURRENT  
 50A/DIV.



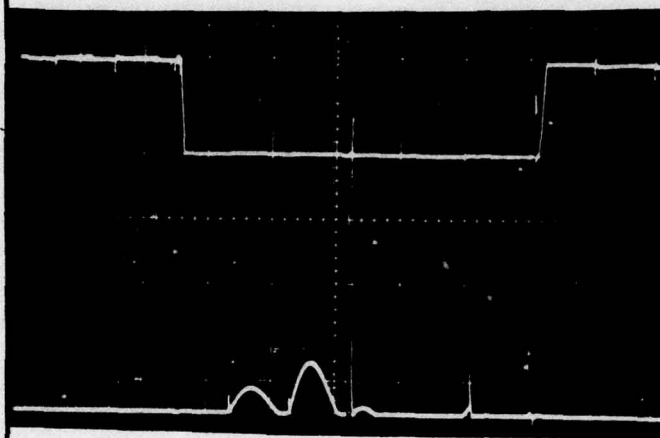
11KW, PF=0.8



20.6 KW, PF=0.8

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DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0009	PAGE JOB NO. DESIGN DATA	PAGE 51
	TITILE		DATE 5/5/78
		PREPARED CORY	
		CHECKED	
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T- THYRISTOR VOLTAGE

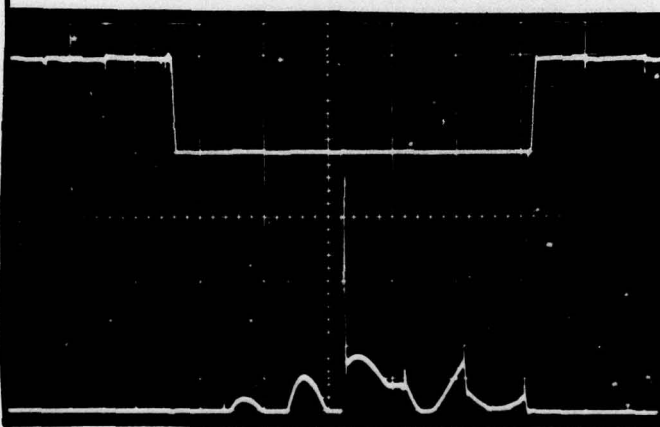
200V / DIV.

NO LOAD

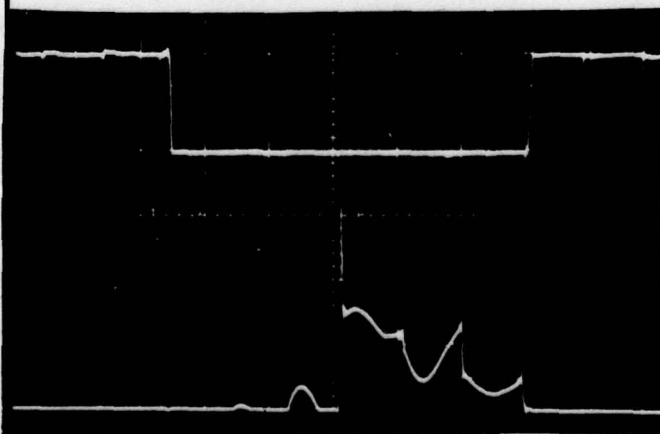
T- CURRENT

50A / DIV.

0.5MS / DIV.



11KW, PF = 0.8



20.6KW, PF = 0.8

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GENERAL MOTORS CORPORATION

REPORT NO.

ITEM No

0009

PAGE

JOB NO.

DESIGN DATA

52

TITLE

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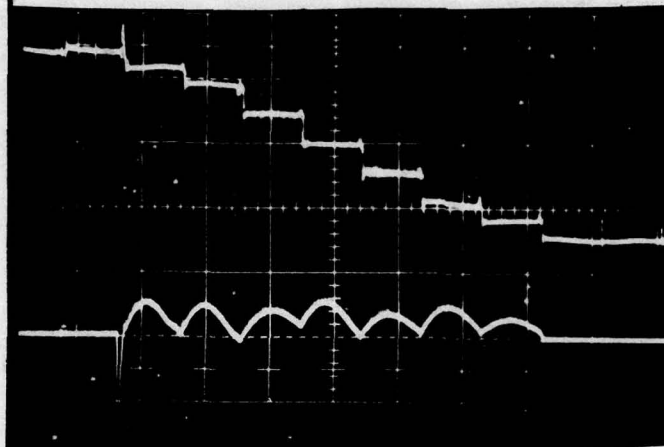
CORRY 5/5/79

DATE

CHECKED

APPROVED

STEP VOLTAGES AND CURRENTS - 60HZ, THREE PHASE



PC. 3 2 1 0 1 2 3

LEFT SIDE STEP  
VOLTAGE

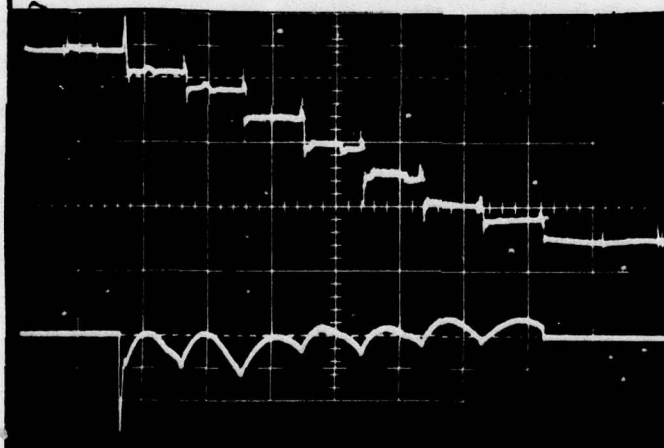
100V/DIV.

NO LOAD

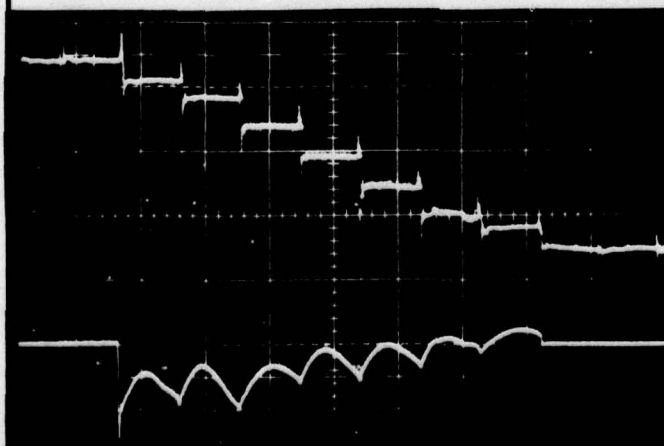
STEP CURRENT

100A/DIV.

0.5MS/DIV.



11KW, PF=0.8

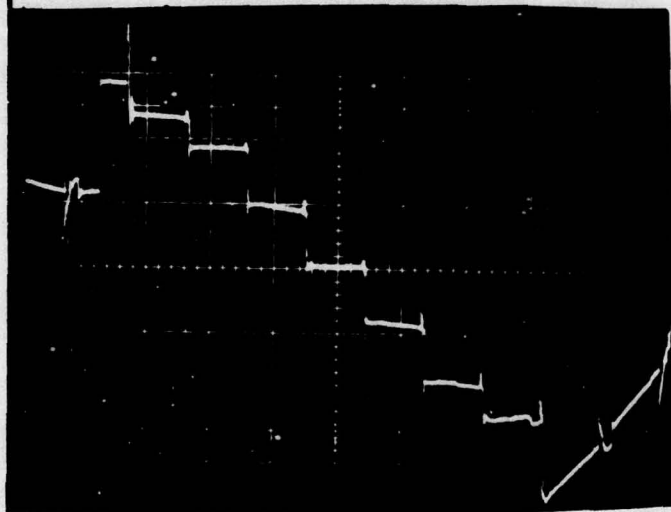


20.6 KW, PF=0.8

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DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0009	PAGE JOB NO. DESIGN DATA	PAGE 53
	TITLE		DATE 5/5/75
		PREPARED CORRY	
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AUTOTRANSFORMER STEP VOLTAGES 60 HZ, 3 PHASE



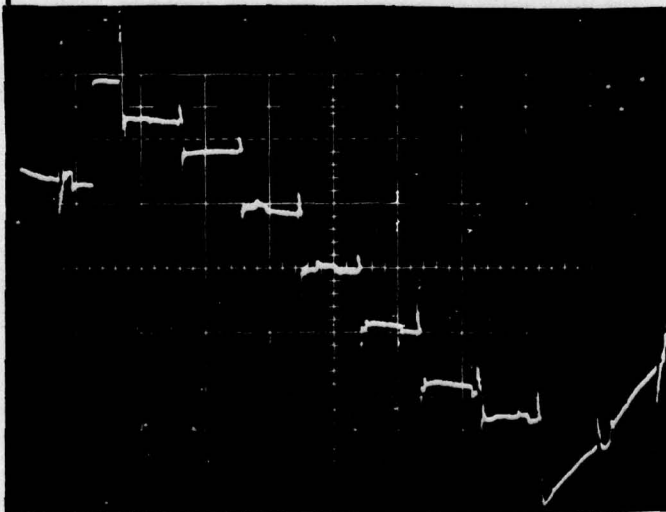
Y STEP FUNCTION

P.C.  
-3  
-2  
-1  
-0  
-1  
-2  
-3

NO LOAD

50V/DIV.

0.5MS/DIV.



11 KW, PF=0.8

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REPORT NO.  
ITEM NO.  
0009.

PAGE JOB NO.  
DESIGN  
DATA

PAGE  
54

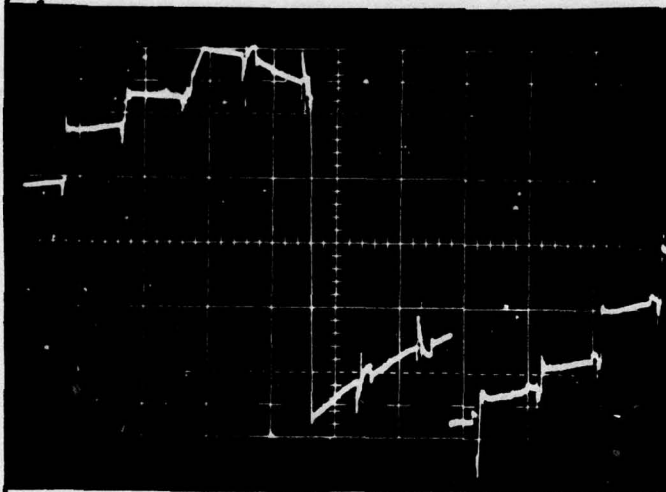
TITLE

PREPARED CORRY DATE 5/5/75

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AUTOTRANSFORMER STEP VOLTAGES 60 HZ, 3 PHASE

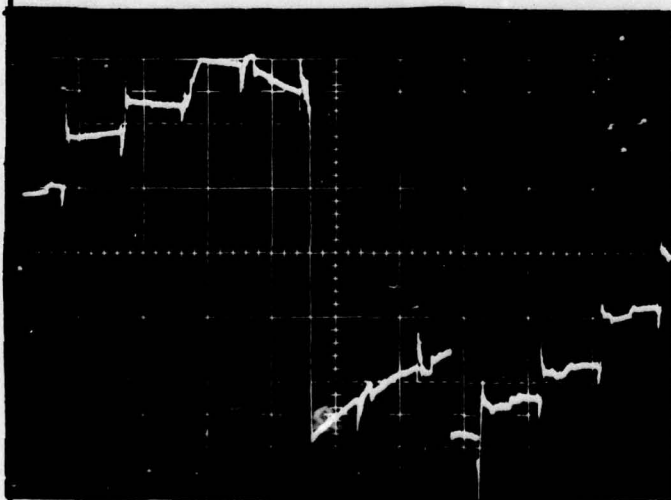


X STEP FUNCTION

NO LOAD

50V/DIV.

0.5ms/DIV.

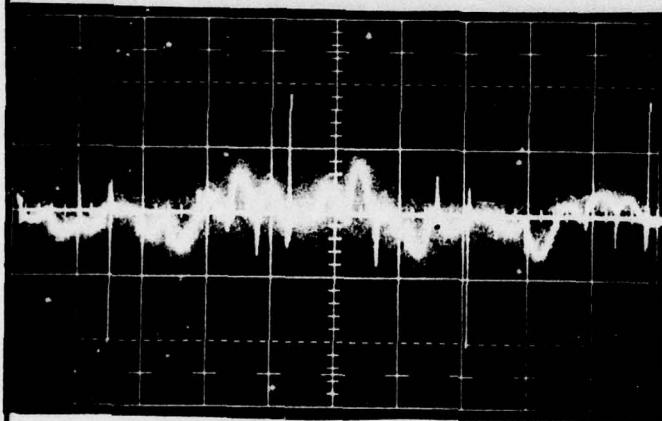


11KW, PF=0.8

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	TITLE		PREPARED CORY	DATE 5/8/75
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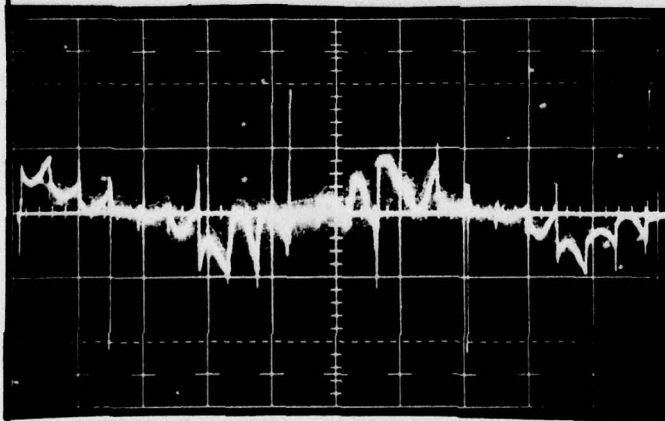
STEP TRANSFORMER CURRENT 60HZ, THREE PHASE



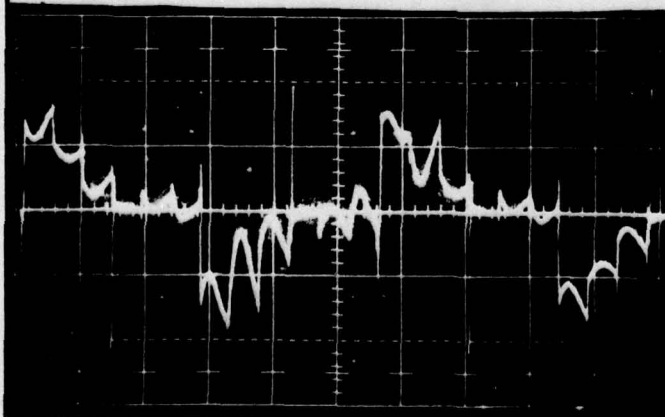
NO LOAD

50 A / DIV.

1 MS / DIV.



11 KW, PF=0.8



20.6 KW, PF=0.8

DISTRIBUTION:

TITLE

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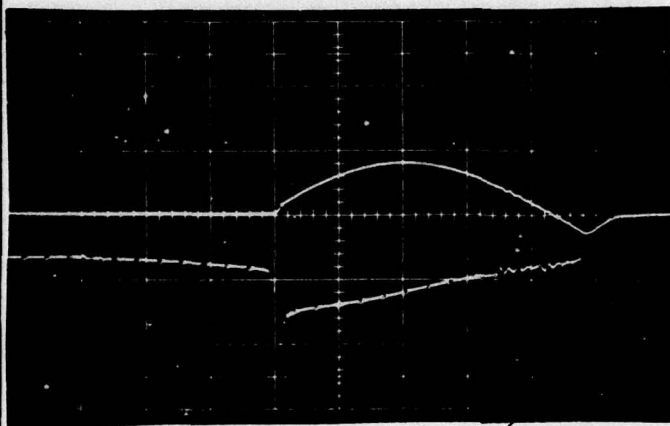
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REVERSE BIAS TURN-OFF TIMES 60HZ, THREE PHASE

20.6KW PF=0.8 LOADS PAGES 11-17



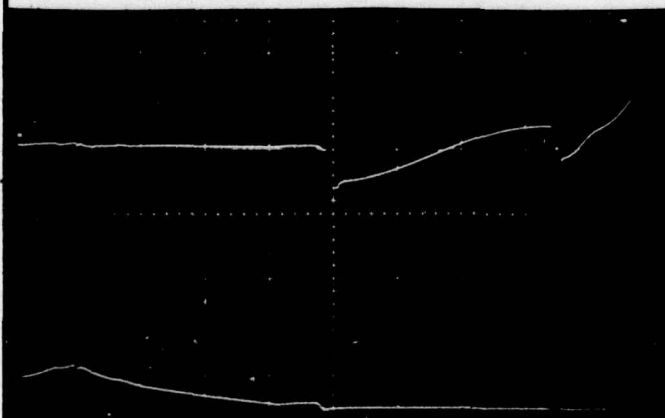
POWER CENTER  
P<sub>T</sub> TURN OFF

BY-PASS DIODE CURRENT  
50A/DIV.

REVERSE BIAS VOLTAGE  
5V/DIV.

5μSEC/DIV.

T - TURN-OFF



REVERSE BIAS VOLTAGE  
20V/DIV.

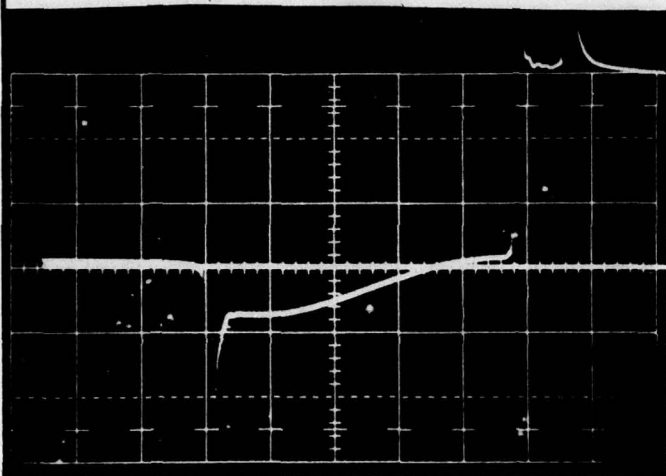
5μSEC/DIV.

ANODE CURRENT  
50A/DIV.

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TITLE

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STEP COMMUTATING  
THYRISTOR L53  
TURN-OFF

20V/DIV.

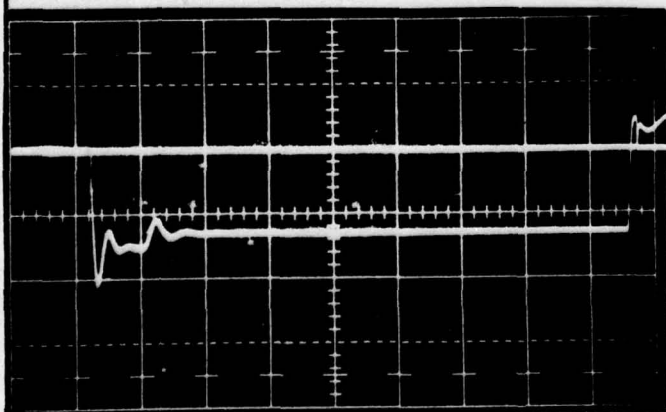
5μSEC/DIV.



STEP COMMUTATING  
THYRISTOR L5A  
TURN-OFF

20V/DIV.

5μSEC/DIV.



STEP THYRISTOR L0  
TURN-OFF

100V/DIV.

50μSEC/DIV.

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GENERAL MOTORS CORPORATION

REPORT NO.  
ITEM NO.  
0009DESIGN  
DATA

58

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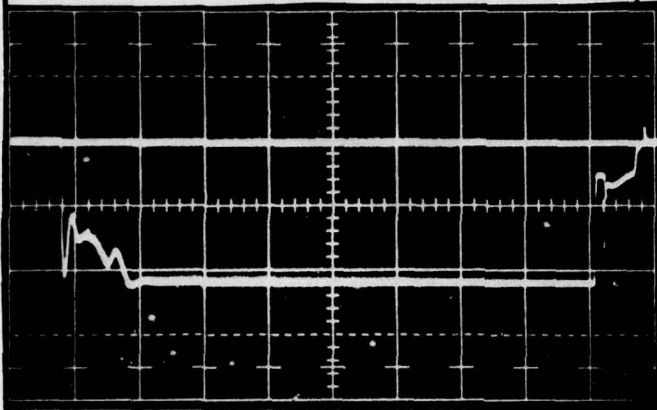
CORY

DATE

5/8/75

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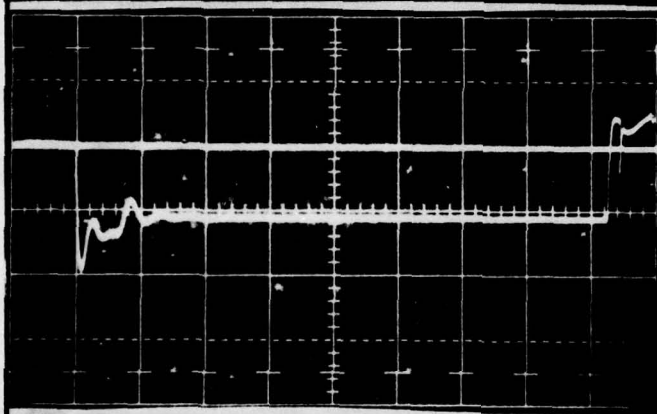
APPROVED



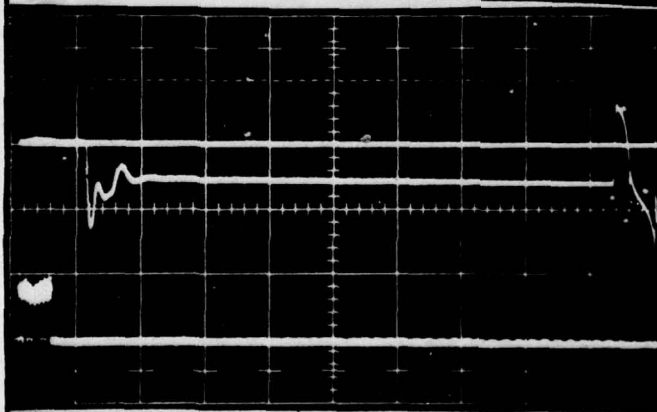
STEP THYRISTOR L<sub>1</sub>  
TURN-OFF

100V/DIV

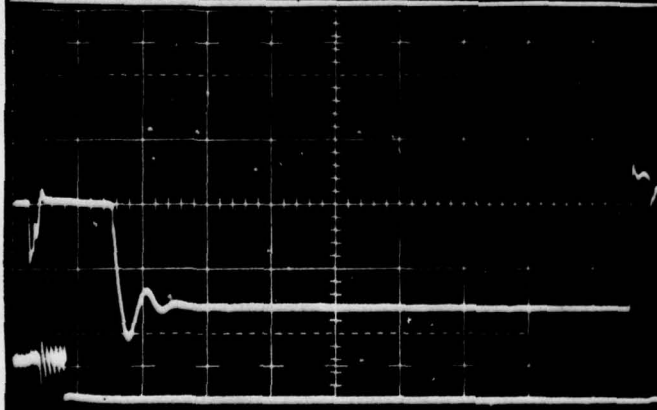
50μSEC/DIV.



STEP THYRISTOR L<sub>2</sub>  
TURN-OFF



STEP THYRISTOR L<sub>3</sub>  
TURN-OFF

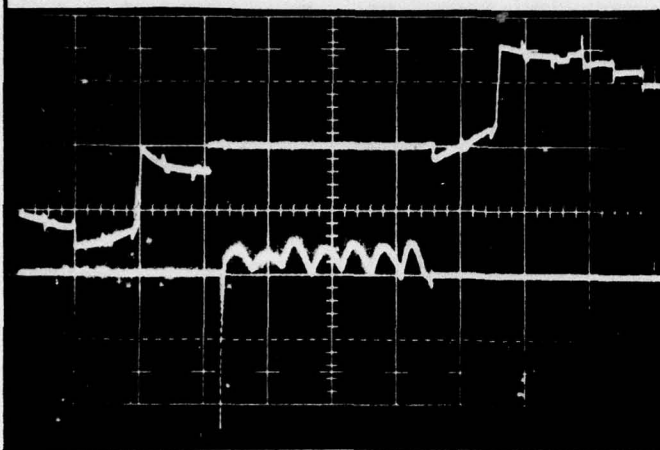


STEP THYRISTOR L<sub>4</sub>  
TURN-OFF

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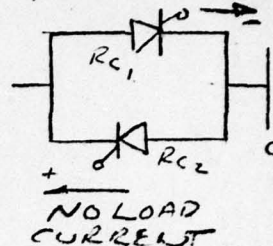
PHASE SELECTOR  $R_C$   
TURN-OFF

200V/DIV.

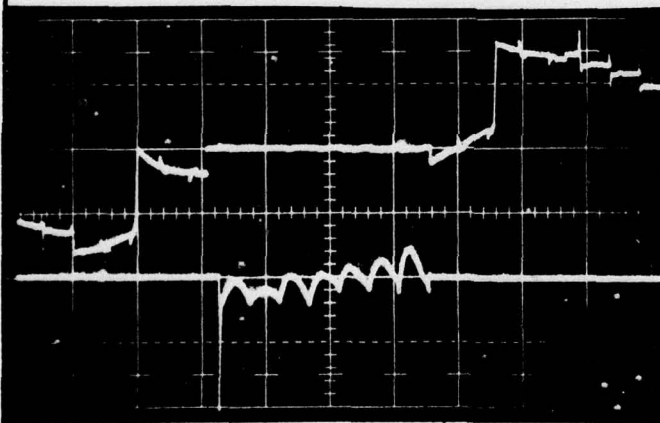
100A/DIV.

1 ms/DIV.

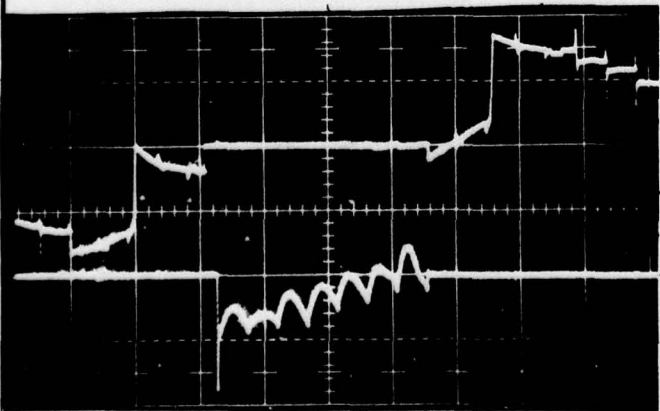
P.C. TURN-OFF PULSE



P.F. CORRECTED  
BOTTOM SCR  
REV. BIASED  
WHEN  $P_C^-$  TURNS  
ON



11KW, PF=0.8



20.6 KW, PF=0.8

REVERSED BIASED FOR 400  
μSEC. WHEN  $P_C^-$  TURNS-ON

FOR LOW P.F. LAGGING  
LOADS (NEG. CURRENT)  
TOP SCR STARVES OFF.

DISTRIBUTION:

TITLE

PREPARED

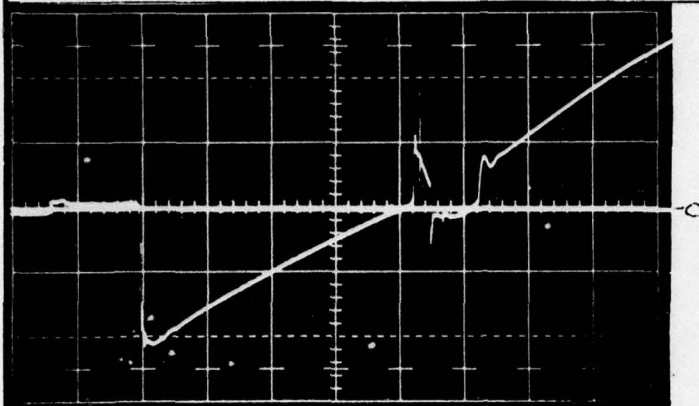
CORY

DATE

5/8/75

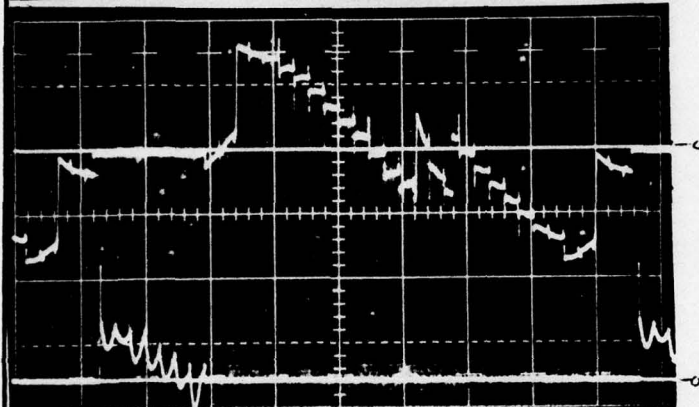
CHECKED

APPROVED

 $R_C$  REVERSE BIAS  
VOLTAGE

20V/DIV.

100μSEC/DIV.

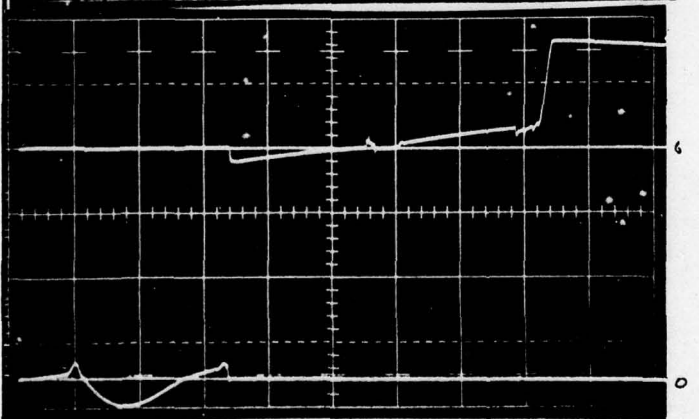


200V/DIV.

2ms/DIV.

CURRENT THRU  $R_C$ 

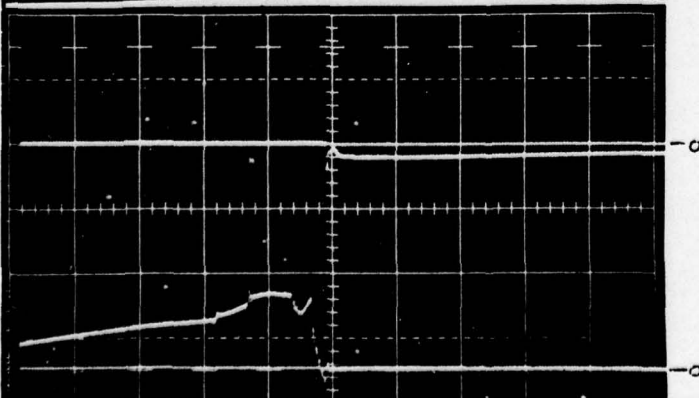
100A/DIV.



VOLTAGE

200V/DIV.

200μSEC/DIV.



CURRENT

100A/DIV.

VOLTAGE

200V/DIV.

20μSEC/DIV.

CURRENT

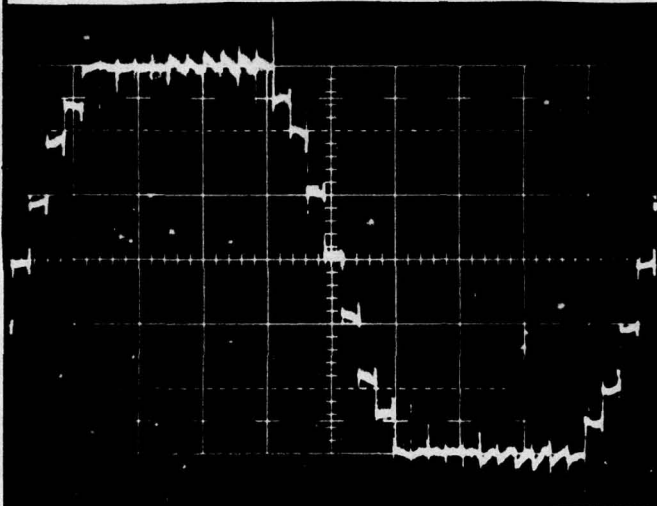
100A/DIV.

DISTRIBUTION:

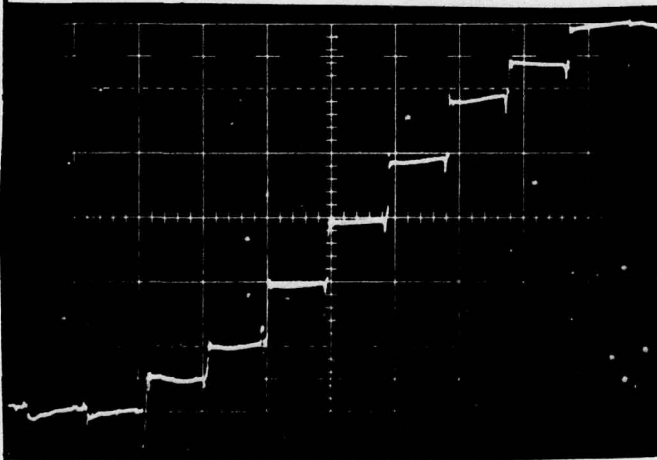
TITLE

PREPARED CORRY 5/8/75  
CHECKED  
APPROVED

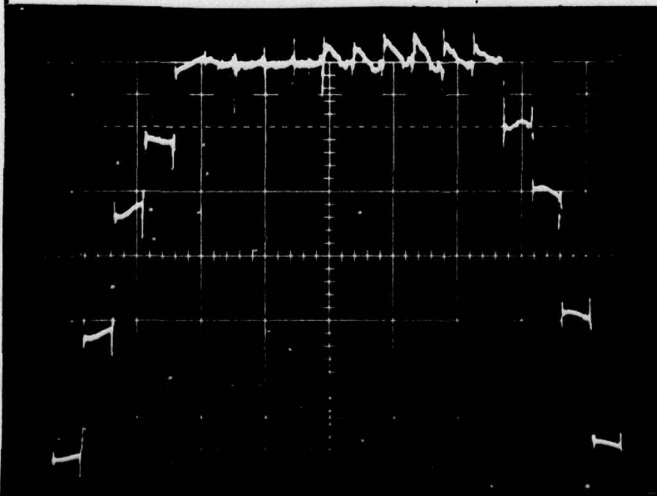
INVERTER BASIC VOLTAGES 60HZ NO LOAD



$V_{c-n}$



0.5 ms/div.



1 ms/div.

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REPORT NO.

ITEM NO.

0009

PAGE

200 NO.

DESIGN

DATA

62

TITLE

PREPARED

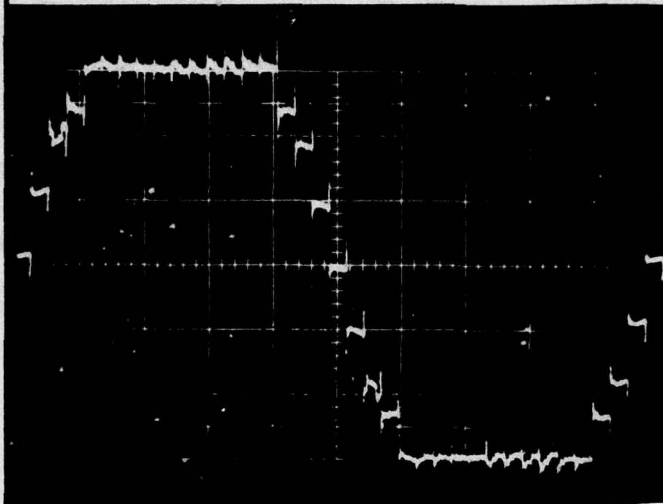
CORRY 5/8/75

DATE

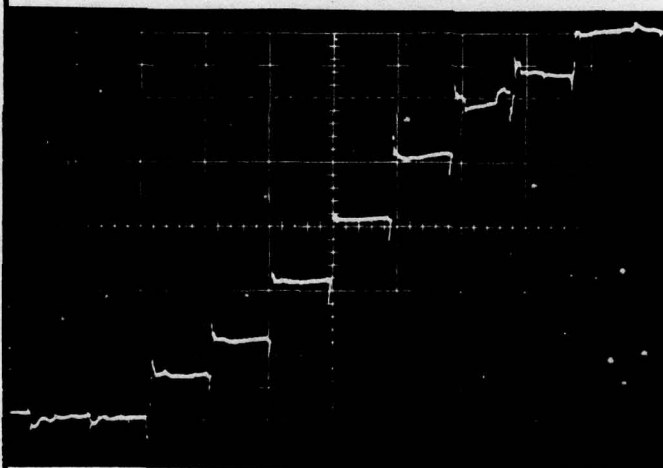
CHECKED

APPROVED

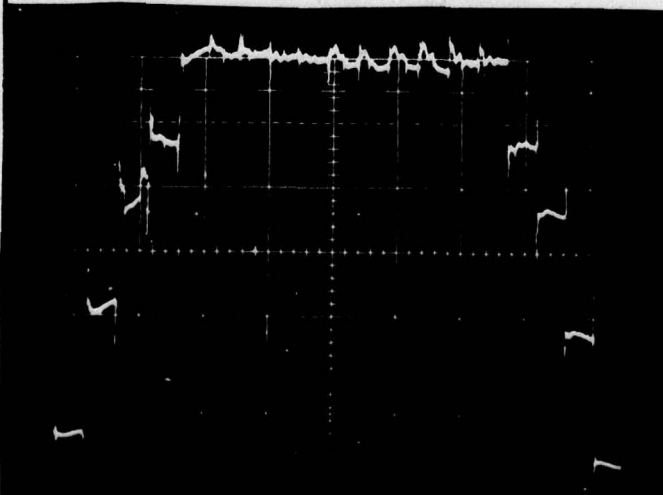
INVERTER BASIC VOLTAGES 60HZ 20.6KW, PF=0.8



V<sub>c-n</sub>



0.5 ms/DIV.



1 ms/DIV.

DISTRIBUTION:

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REPORT NO.  
ITEM NO.  
0009

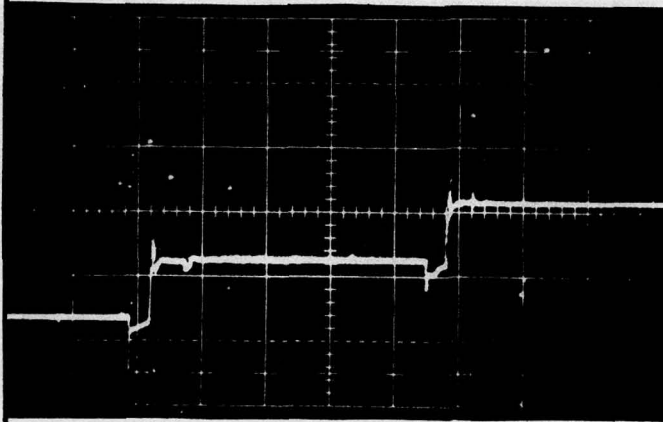
PAGE JOB NO.  
DESIGN  
DATA

PAGE  
63

TITLE

PREPARED CORRY 5/8/75 DATE  
CHECKED  
APPROVED

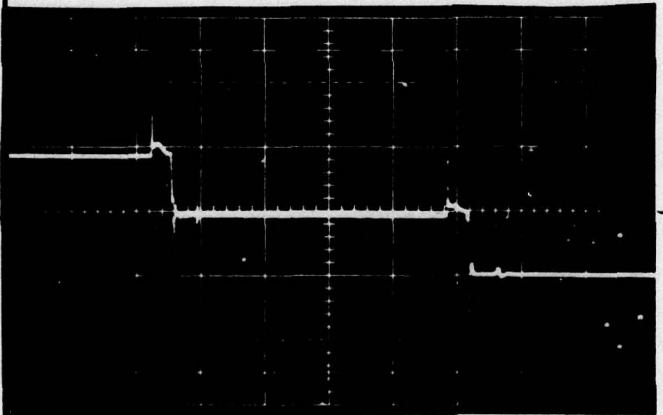
INVERTER BASIC VOLTAGES 60HZ NO LOAD



ASCENDING STEPS  
2, 1, 0

50V/DIV.

100μSEC/DIV.



DESCENDING STEPS  
1, 0, 1



POWER CENTER AND  
STEPS 3, 2

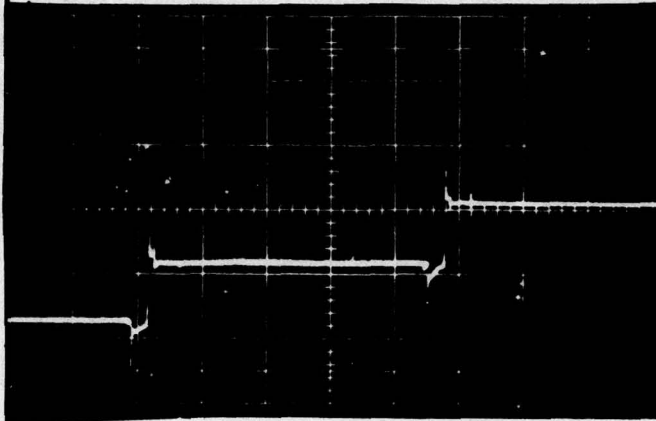
DISTRIBUTION:

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REPORT NO.  
ITEM NO.  
0009PAGE JOB NO.  
DESIGN  
DATAPAGE  
64

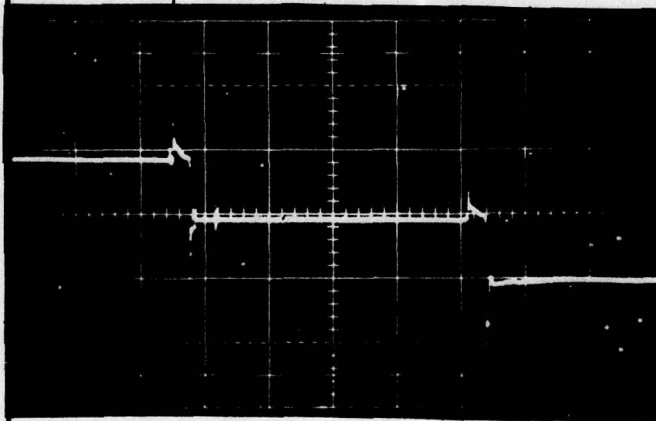
TITLE

PREPARED  
CORRY  
DATE  
5/8/75  
CHECKED  
APPROVEDINVERTER BASIC VOLTAGES 60Hz 16KW, PF=0.8

ASCENDING STEPS

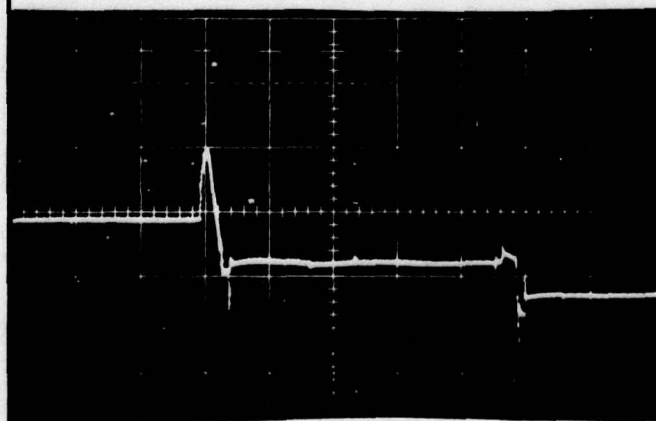
2, 1, 0  
50V/DIV.

100μSEC/DIV.



DESCENDING STEPS

1, 0, 1

POWER CENTER AND  
STEPS 3, 2

DISTRIBUTION:

DELCO ELECTRONICS

GENERAL MOTORS CORPORATION

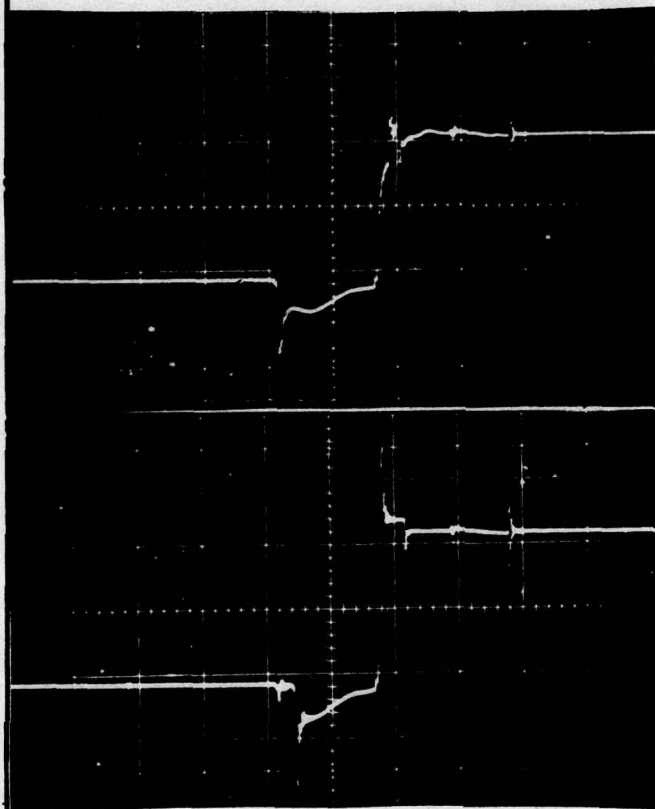
REPORT NO.  
ITEM NO.  
0009

PAGE JOB NO.  
DESIGN  
DATA

PAGE  
65

TITLE

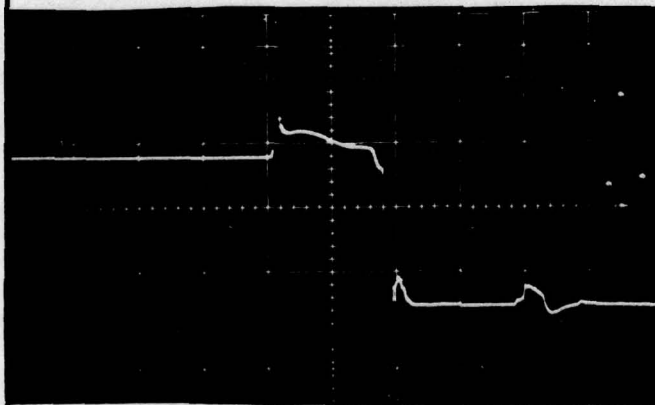
PREPARED CORRY 5/8/75 DATE  
CHECKED  
APPROVED



ASCENDING

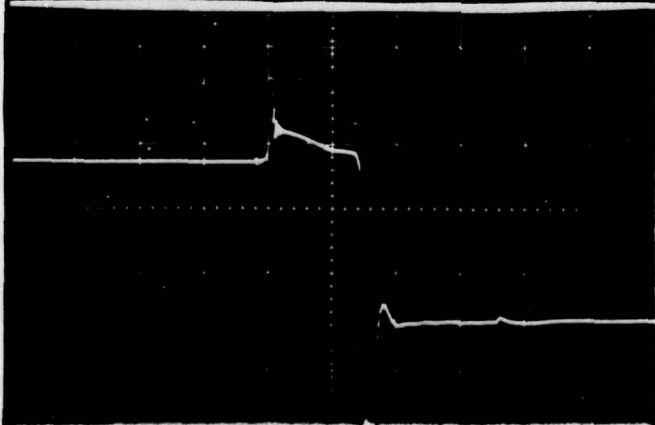
20V / DIV.  
20 μSEC / DIV.

NO LOAD



DESCENDING

NO LOAD

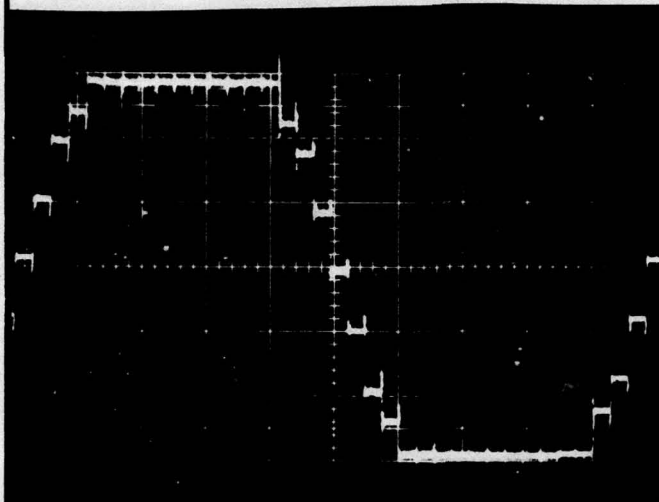


16KW, PF=0.8

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DELCO ELECTRONICS GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0009	PAGE DESIGN DATA	PAGE 66
	TITLE		DATE 5/8/75
		PREPARED CORRY	
		CHECKED	
		APPROVED	

# 60 HZ THREE PHASE VOLTAGES

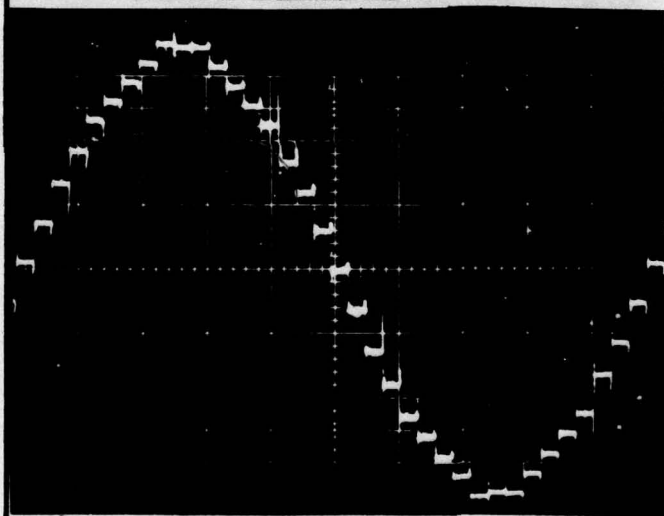


L-T-N VOLTAGE  
 $V_{a-n}$

NO OUTPUT CAPACITANCE

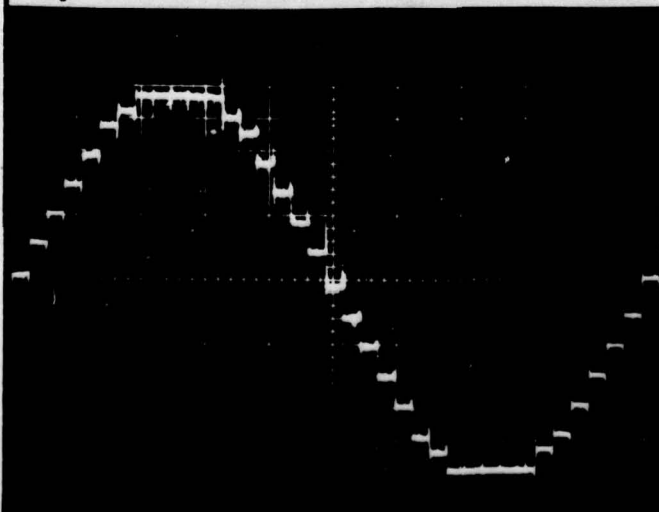
NO LOAD

50V / DIV.



L-T-N VOLTAGE  
ON LOAD SIDE  
OF TRIPLEN ATTENU-  
ATOR

THD = 5.65%



L-T-L VOLTAGE

100V / DIV.

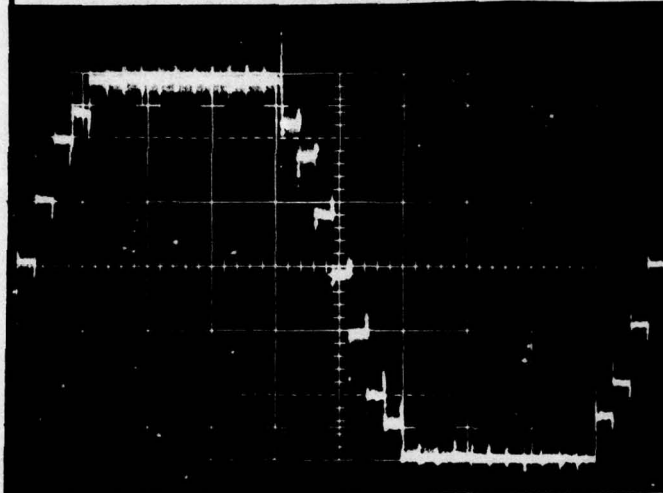
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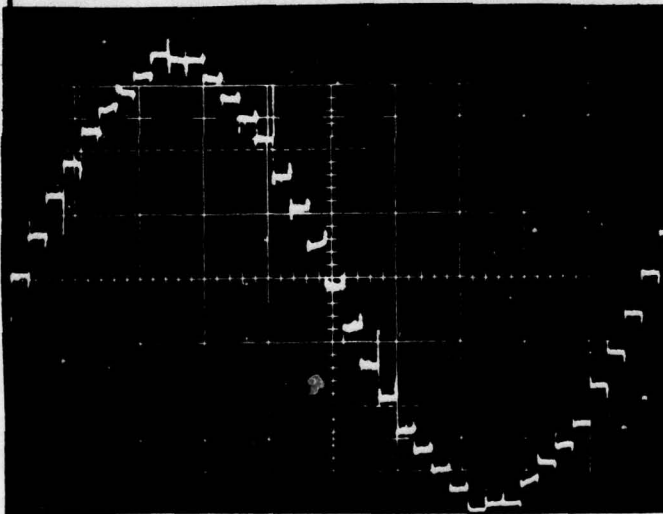
APPROVED

60 HZ THREE PHASE VOLTAGESL-T-N VOLTAGE  
 $V_{a-n}$ 

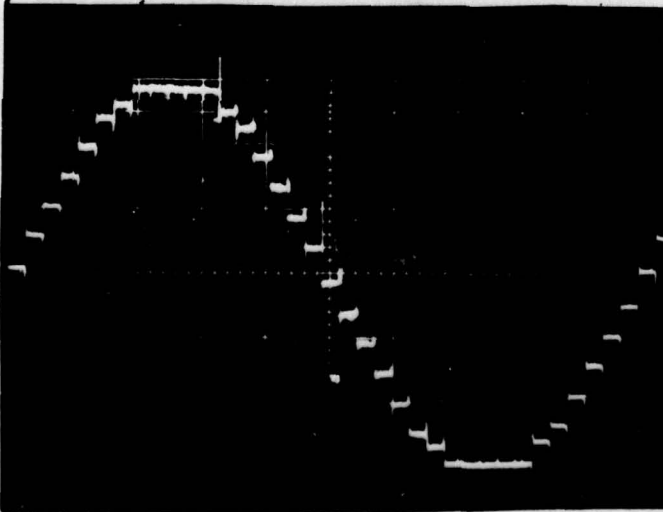
NO OUTPUT CAPACITANCE

16KW, PF = 0.8

50V/DIV.

L-T-N VOLTAGE ON  
LOAD SIDE OF  
TRIPLIN ATTENUATOR

THD = 7%



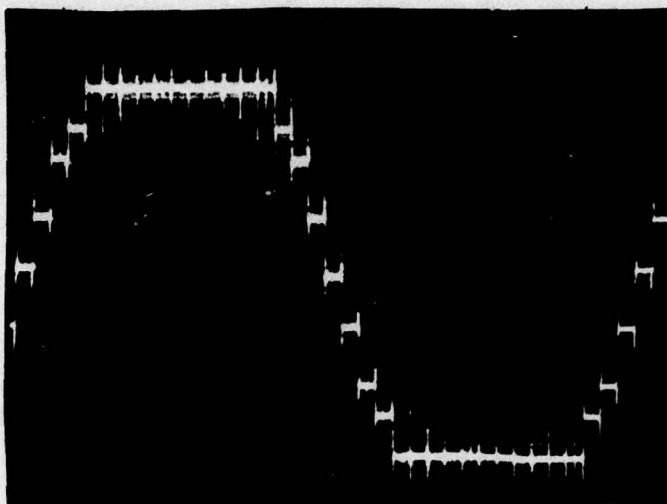
L-T-L VOLTAGE

100V/DIV.

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PREPARED  
CORR-1 5/8/75  
DATE  
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BASIC L-T-N  
VOLTAGE WITH  
INTENSITY  
TURNED UP  
TO SHOW  
HIGHER FRE-  
QUENCY  
HARMONICS

HARMONIC NUMBER	FREQUENCY HZ	PERCENT OF FUNDAMENTAL		
		MEASURED * L-T-N	MEASURED * L-T-L	COMPUTED L-T-N OR L-T-L
1	60	100.0	100.0	100.0
3	180	0.1	—	18.63
5	300	0.8	0.8	0.98
7	420	1.5	1.5	1.46
9	540	—	—	3.24
11	660	0.8	0.8	0.96
13	780	0.45	0.44	0.21
15	900	—	—	1.17
17	1020	0.87	0.87	0.65
19	1140	0.58	0.60	0.54
21	1260	—	—	0.86
23	1380	0.40	0.40	0.16
25	1500	0.37	0.36	0.43
29	1740	0.30	0.30	0.15
31	1860	—	0.1	0.12
33	1980	—	—	1.63
35	2100	3.0	3.0	2.88
37	2220	2.5	2.6	2.71
39	2340	—	—	1.37
41	2460	—	—	0.10

\* MEASUREMENTS MADE AT OUTPUT OF TRIPLEX  
ATTENUATOR. LOAD = 11KW, PF=1.0. IMPD CAP L-T-N  
MEASURED THD=5.3%. COMPUTER DESIGNED WAVEFORM THD=5.6%

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GENERAL MOTORS CORPORATION

REPORT NO.  
ITEM NO.  
0009

PAGE JOB NO.  
DESIGN  
DATA

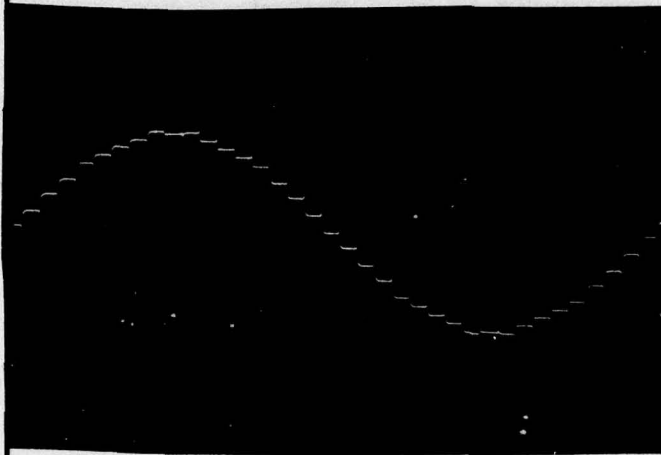
PAGE  
69

TITLE

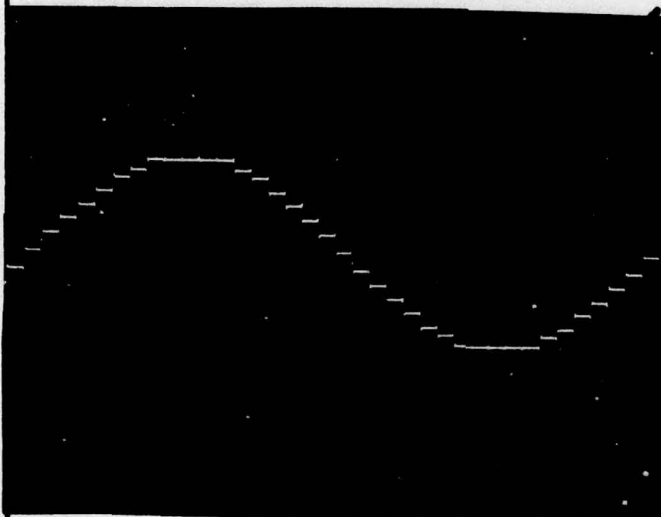
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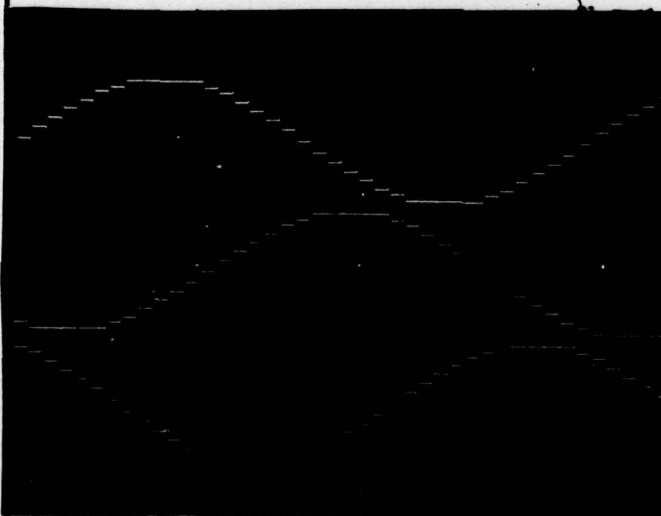
APPROVED



UNFILTERED LINE-TO-  
NEUTRAL VOLTAGE



UNFILTERED LINE-TO-  
LINE VOLTAGE

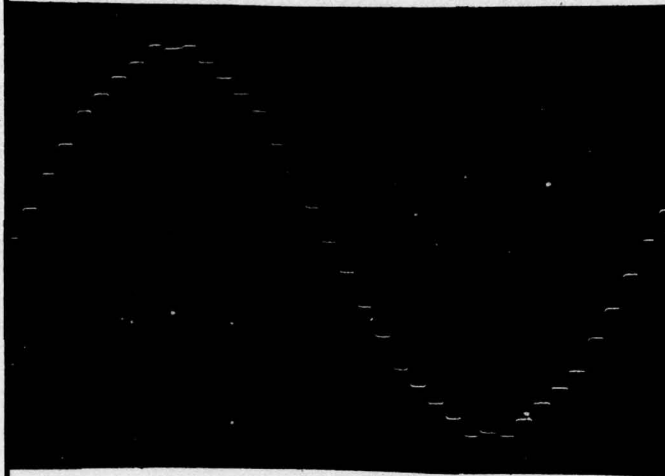


THREE PHASE L-T-L  
VOLTAGES

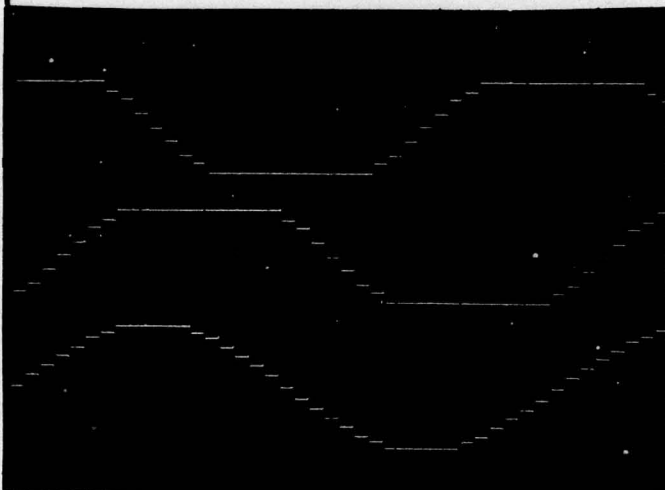
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APPROVED



UNFILTERED L-T-N  
VOLTAGE AT OUTPUT  
OF TRIPLEX ATTENUATOR



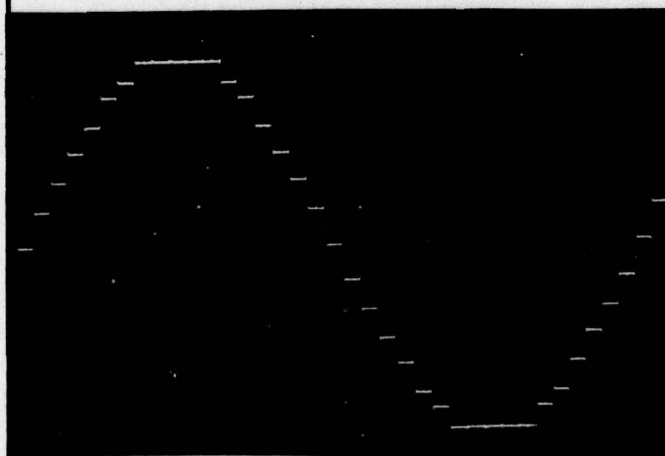
$V_{an}$

$V_{bn}$

$V_{cn}$

$$V_{an} + V_{bn} = V_{ab}$$

L-T-N VOLTAGES AND  
RESULTANT L-T-L  
VOLTAGE



UNFILTERED L-T-L  
VOLTAGE

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GENERAL MOTORS CORPORATION

REPORT NO.  
ITEM NO.  
0009

PAGE JOB NO.

DESIGN  
DATA

PAGE

71

TITLE

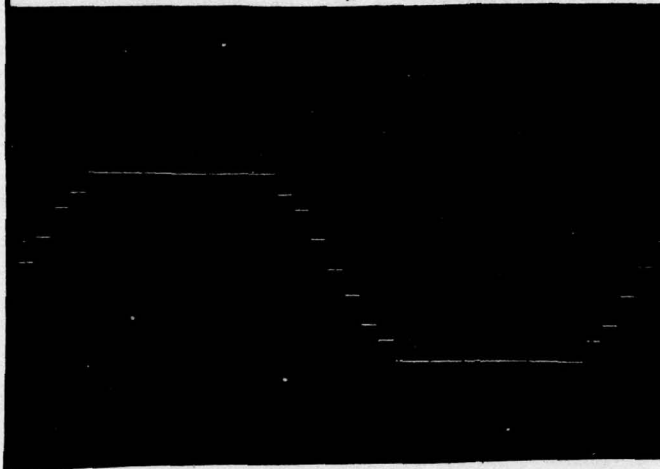
PREPARED

CORRY 5/8/75

DATE

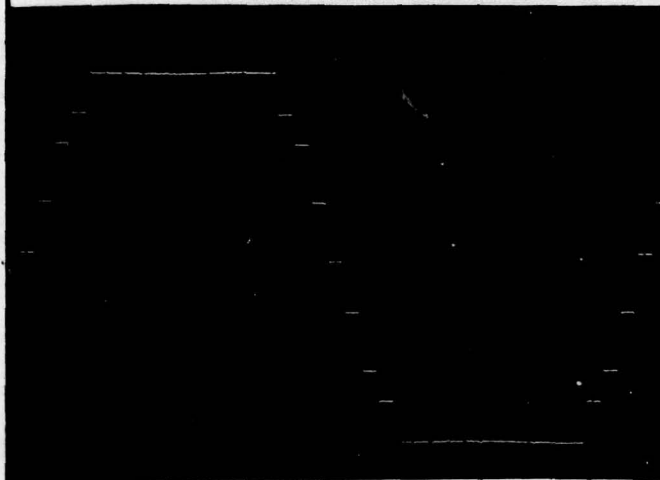
CHECKED

APPROVED

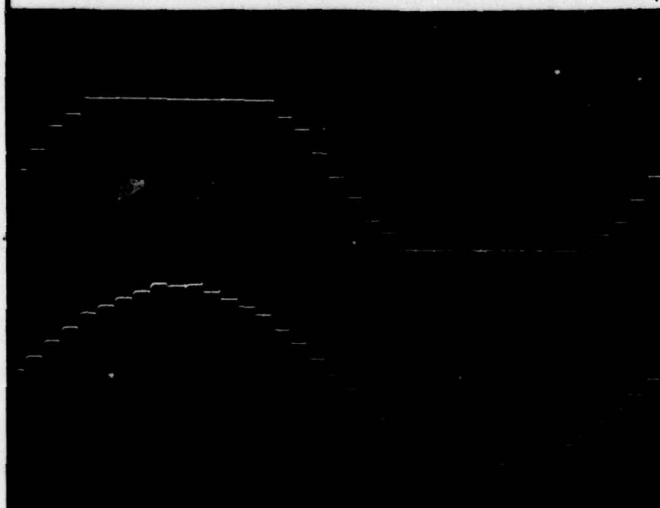


PHOTOGRAPHS TAKEN AT  
60 HZ, 11KW, PF=1.0 LOAD

INVERTER BASIC  
LINE-TO-NEUTRAL  
VOLTAGE



BASIC LINE-TO-NEUTRAL  
VOLTAGE EXPANDED  
IN AMPLITUDE



VOLTAGE INTO TRIPLEN  
ATTENUATOR

L-T-N VOLTAGE AT  
OUTPUT OF TRIPLEN  
ATTENUATOR

DISTRIBUTION:

TITLE

PREPARED

CORRY 5/5/75

DATE

CHECKED

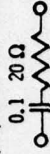
APPROVED

# THYRISTOR AND DIODE VOLTAGES AND CURRENTS

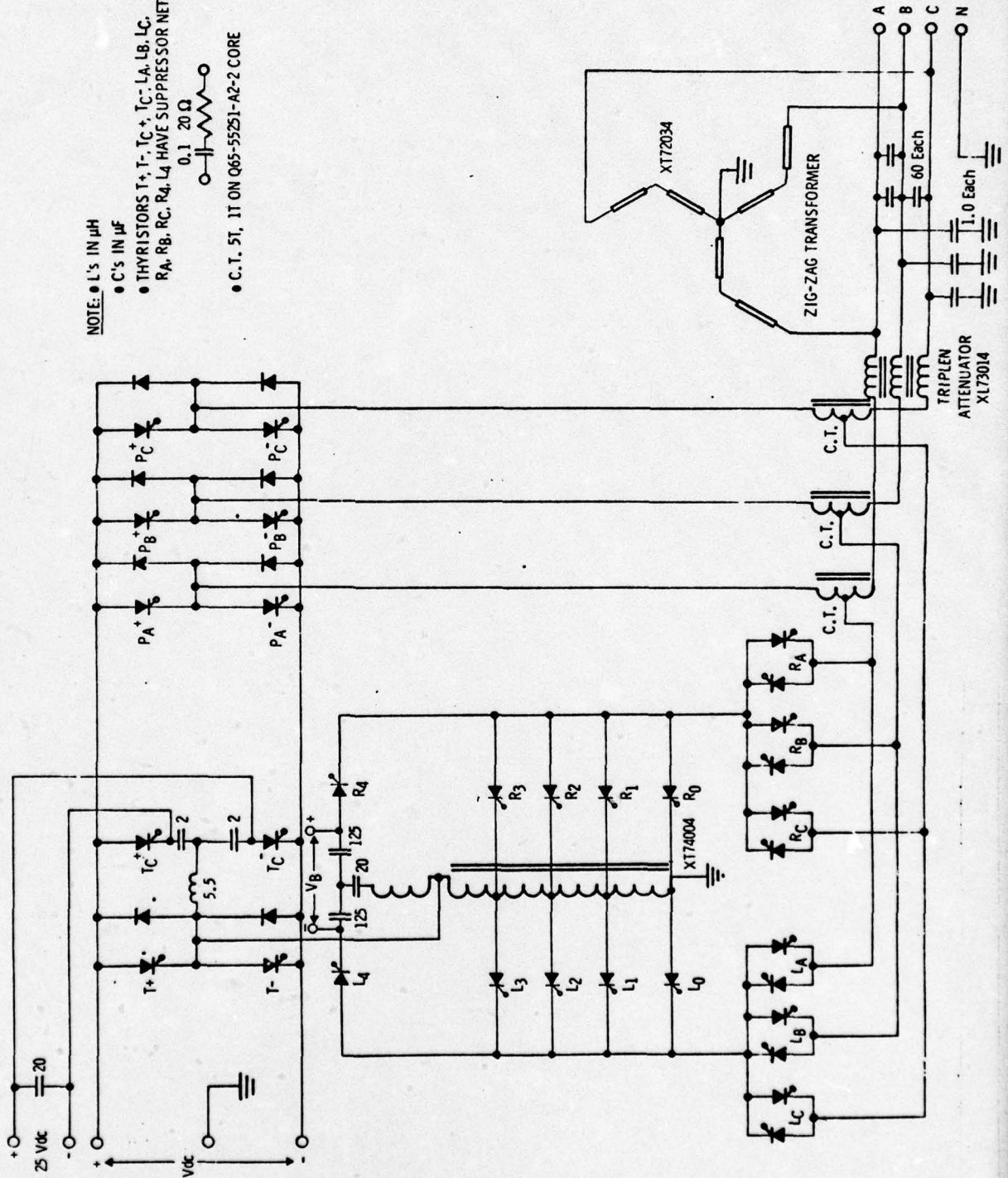
NOTE: L's IN  $\mu H$

C's IN  $\mu F$

• THYRISTORS T<sub>1</sub>, T<sub>2</sub>, T<sub>3</sub>, T<sub>4</sub>; L<sub>A</sub>, L<sub>B</sub>, L<sub>C</sub>,  
R<sub>A</sub>, R<sub>B</sub>, R<sub>C</sub>, R<sub>4</sub>, L<sub>4</sub> HAVE SUPPRESSOR NETWORKS:



• C.T. 5T, 1T ON Q65-55251-A2-2 CORE



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TITLE

PREPARED

CORRY 5/8/75

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APPROVED

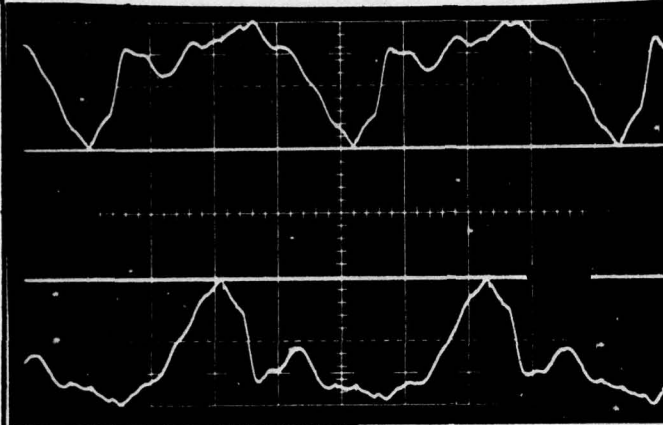
FREQUENCY CONVERTER INPUT CURRENTS  
(P.F. CORRECTED) CIRCUIT

400 HZ THREE PHASE

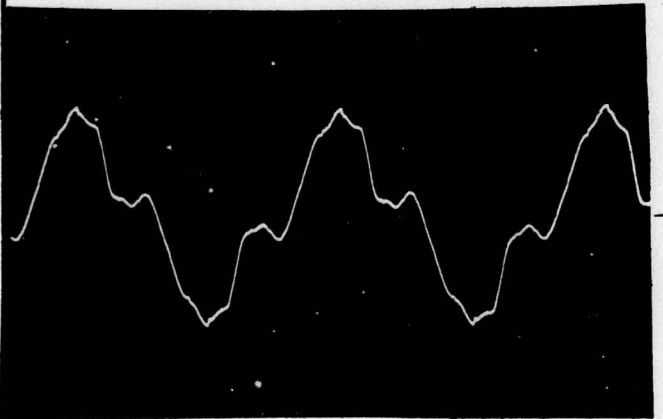
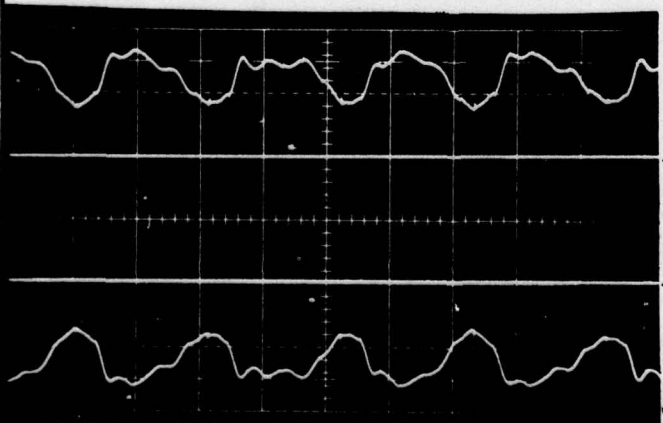
161KW, PF=1.0

↑ 50A/DIV.

← 200μSEC/DIV.



NEUTRAL CURRENT

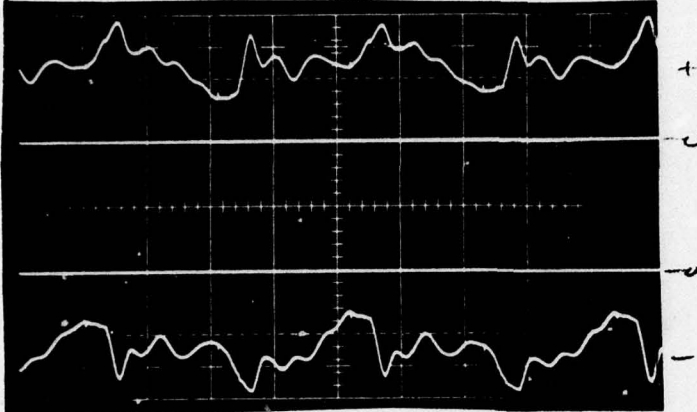
± INPUT CURRENTS  
WITH NEUTRAL  
NOT CONNECTED.

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APPROVED

FREQUENCY CONVERTER INPUT CURRENTS

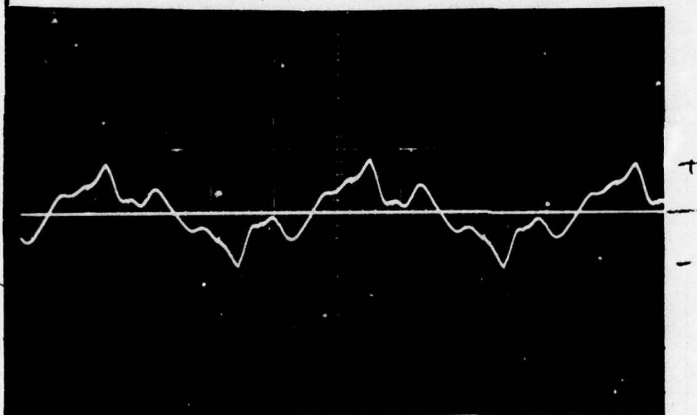


400 HZ THREE PHASE

16 KW, PF = 0.8

↓ 50 A/DIV.

↔ 200 μSEC/DIV.



NEUTRAL CURRENT



± INPUT CURRENTS  
WITH NEUTRAL  
NOT CONNECTED

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DELCO ELECTRONICS

GENERAL MOTORS CORPORATION

REPORT NO.

ITEM NO.

0009

PAGE

JOB NO.

DESIGN

DATA

PAGE

75

TITLE

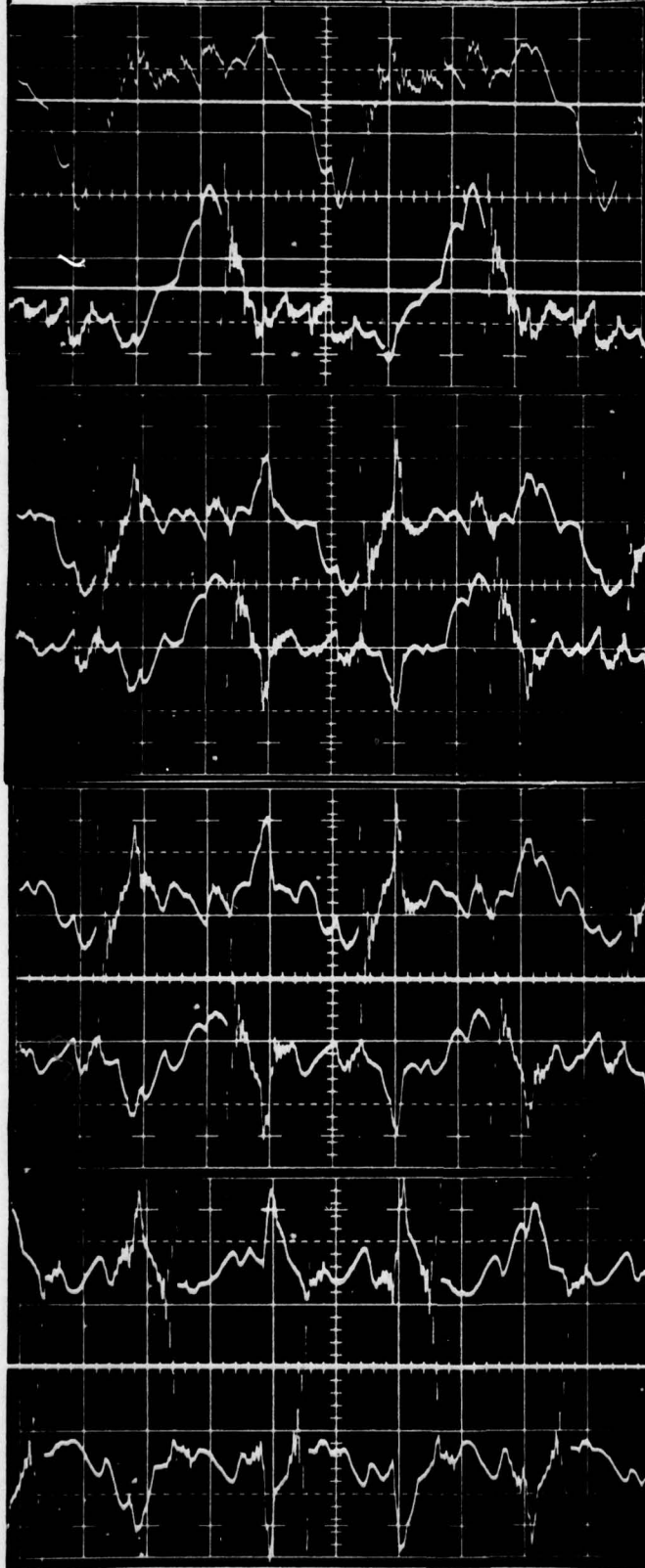
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CORRY 5/8/75

DATE

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400 HZ THREE PHASE DC INPUT CURRENTS

50A/DIV.

200μs/DIV.

NO LOAD

11KW, PF=0.8

16KW, PF=0.8

20.6KW, PF=0.8

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PREPARED

CORY

DATE

5/8/75

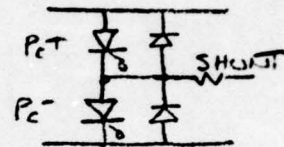
CHECKED

APPROVED

POWER CENTER THYRISTOR VOLTAGES AND CURRENTS.  
400HZ, THREE PHASE (P.F. CORRECTED)

POWER CENTER P<sub>c</sub><sup>-</sup>  
THYRISTOR VOLTAGE  
200V/DIV.

THYRISTOR & DIODE CURRENT  
50A/DIV.

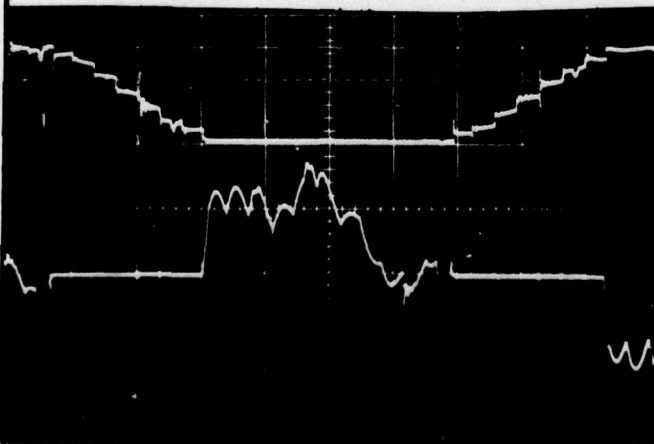
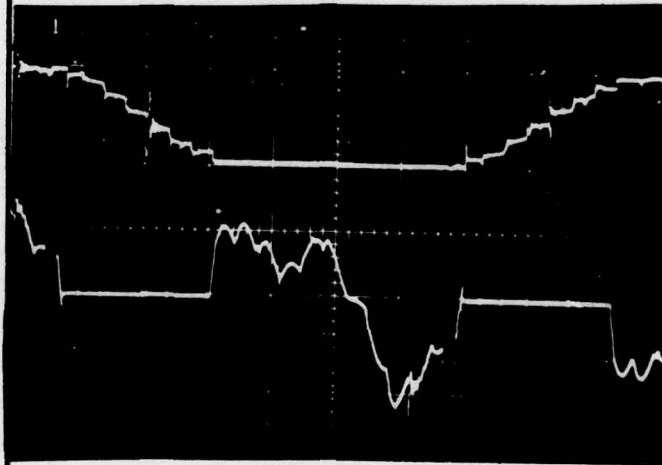


{ BOOST COMMUTATION  
VOLTAGE = 72VDC  
CURRENT = 6AMPS DC  
FOR ALL V&I PICTURES  
JAPANESE C.T. COMMU-  
TATION XFM'R IN. }

NO LOAD

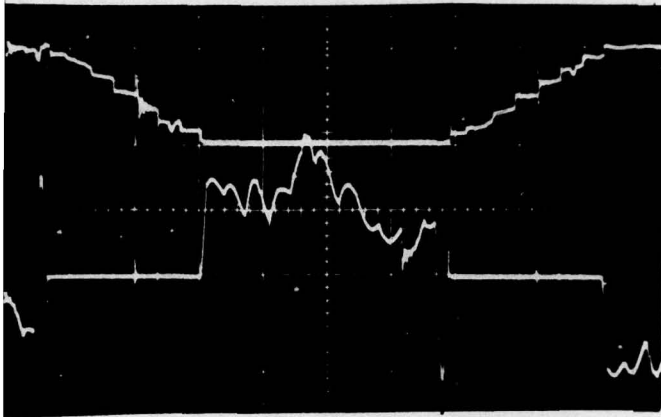
(NOTE: BY PASS DIODE  
PEAK CURRENT = 210 AMPS)

11KW, PF = 0.8

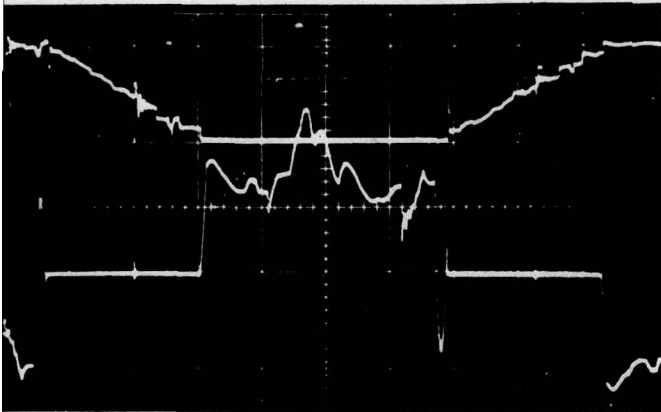


DISTRIBUTION:

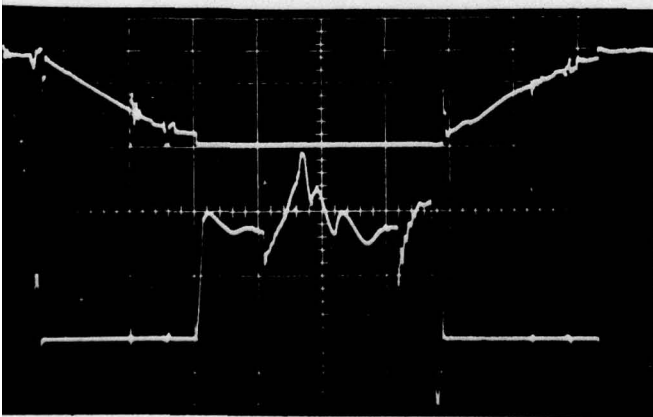
<b>DELCO ELECTRONICS</b> GENERAL MOTORS CORPORATION	REPORT NO. ITEM NO. 0009	PAGE 1	DESIGN DATA	77
	TITLE		PREPARED CORY 5/8/75	DATE
		CHECKED		
		APPROVED		



16KW, PF=0.8



20.6KW, PF=0.8



24.8KW, PF=0.8

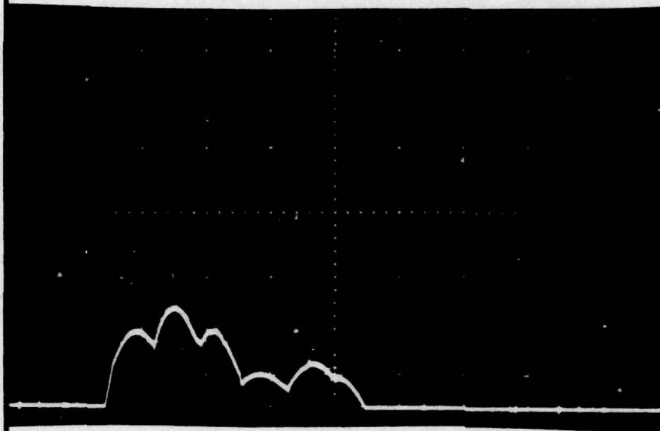
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PREPARED CORRY DATE 5/8/75

CHECKED

APPROVED

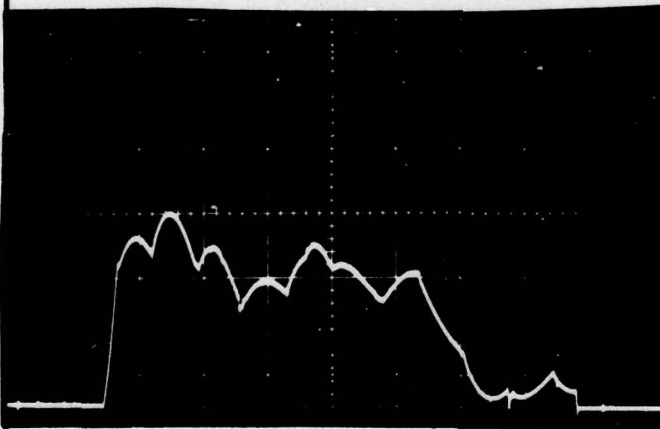
POWER CENTER CURRENT PE 400 HZ THREE PHASE



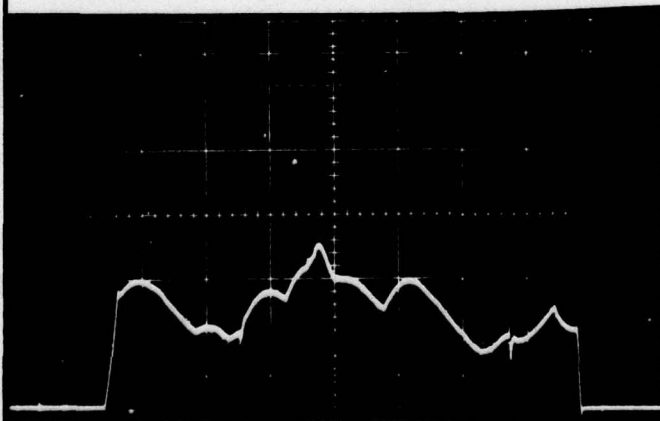
NO LOAD

50A/DIV.

100.μSEC/DIV.



20.6 KW, PF=1.0



20.6 KW, PF=0.8

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DELCO ELECTRONICS

GENERAL MOTORS CORPORATION

ITEM NO.

0009

DESIGN

DATA

79

TITLE

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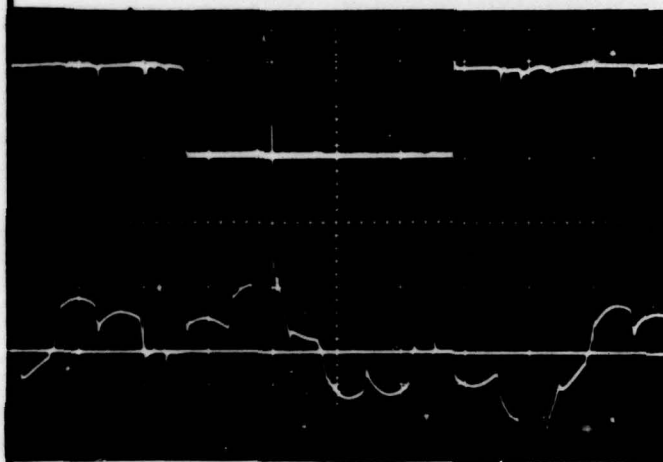
CORY

DATE

5/8/75

CHECKED

APPROVED



T- THYRISTOR VOLTAGE

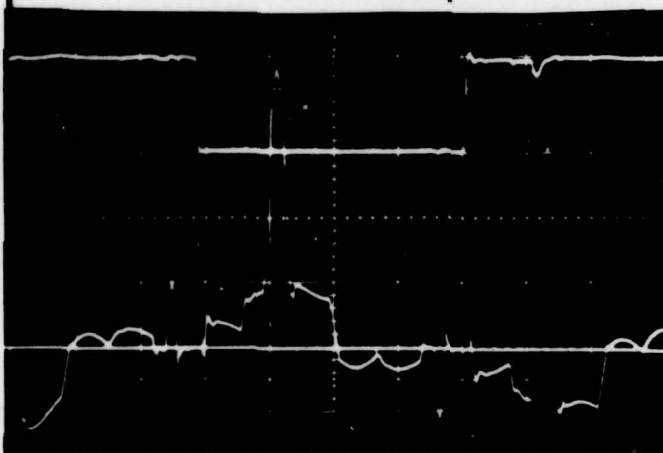
200V/DIV.

NO LOAD

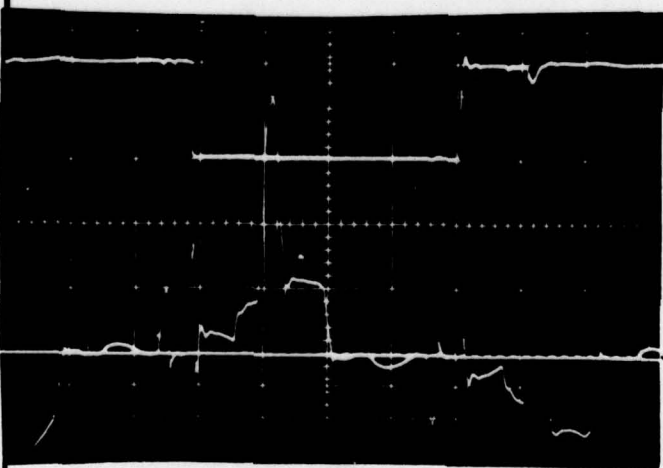
T- CURRENT

50A/DIV.

100μSEC/DIV.



11KW, PF=0.8



16KW, PF=0.8

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DELCO ELECTRONICS

GENERAL MOTORS CORPORATION

REPORT NO.

ITEM NO.

0009

PAGE

JOB NO.

DESIGN  
DATA

WEEK

80

TITLE

PREPARED

CORRY

DATE

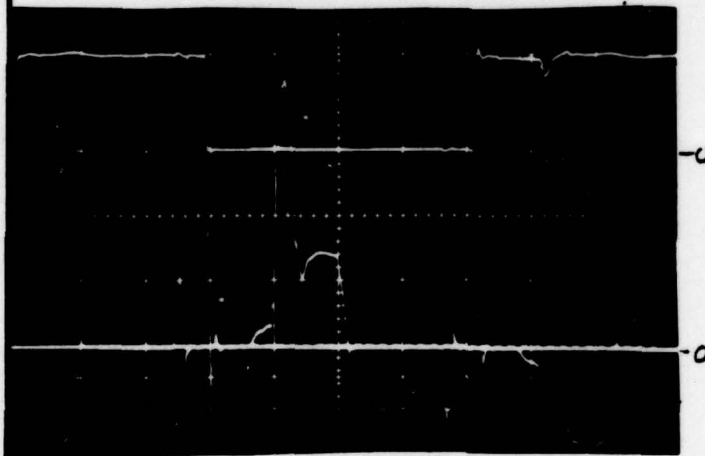
5/8/75

CHECKED

APPROVED

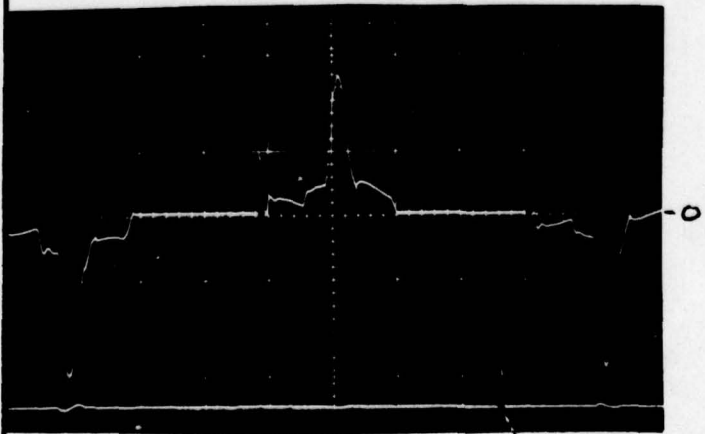


20.6 KW, PF = 0.8



24.8 KW, PF = 0.8

(92 AMPS DC INTO  
INVERTER)



SINGLE PHASE LOAD

5 KW, PF = 0.8 L-T-N

100V/DIV.  
100μSEC/DIV.

T<sub>c</sub> TRIGGER

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DELCO ELECTRONICS

GENERAL MOTORS CORPORATION

REPORT NO.

ITEM NO.

0009

PAGE

JOB NO.

DESIGN

DATA

PAGE

81

TITLE

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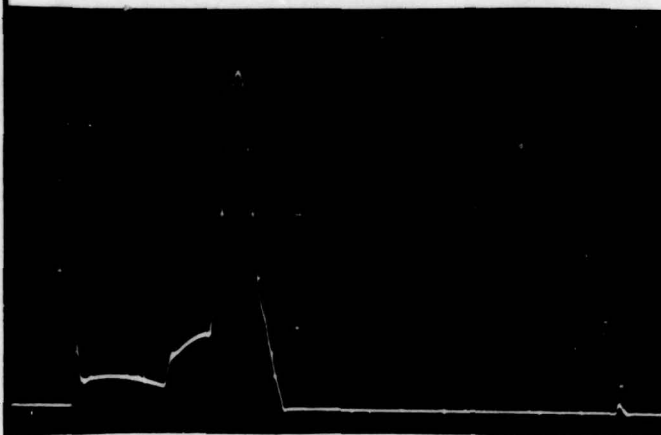
CORR-1 5/8/75

DATE

CHECKED

APPROVED

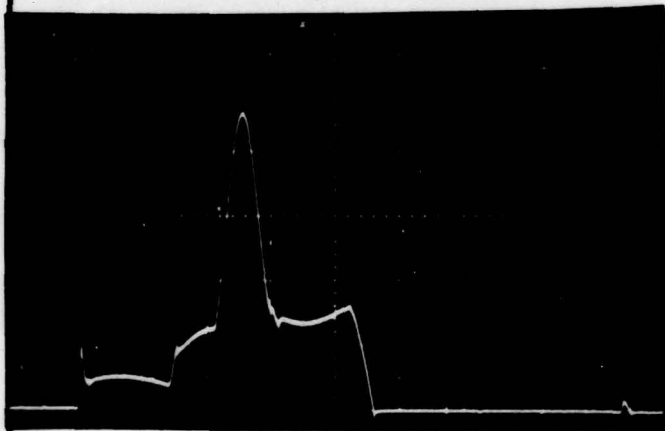
T-CURRENT 400HZ THREE PHASE



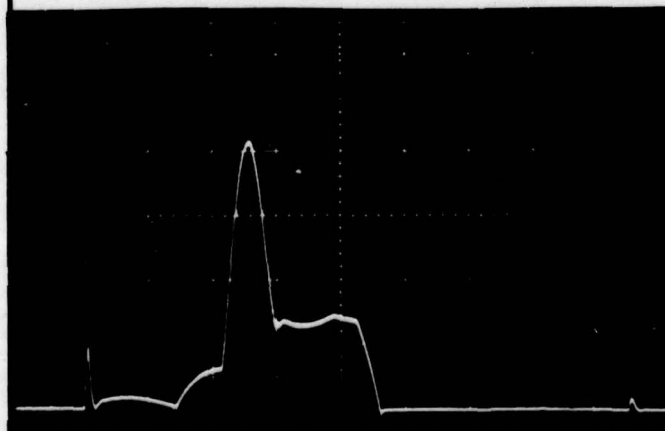
NO LOAD

50A/DIV.

50μSEC/DIV.



20.6KW, PF=1.0



20.6KW, PF=0.8

(2WIRE INPUT; 60MFD  
L-T-L OUTPUT CAPACITANCE)

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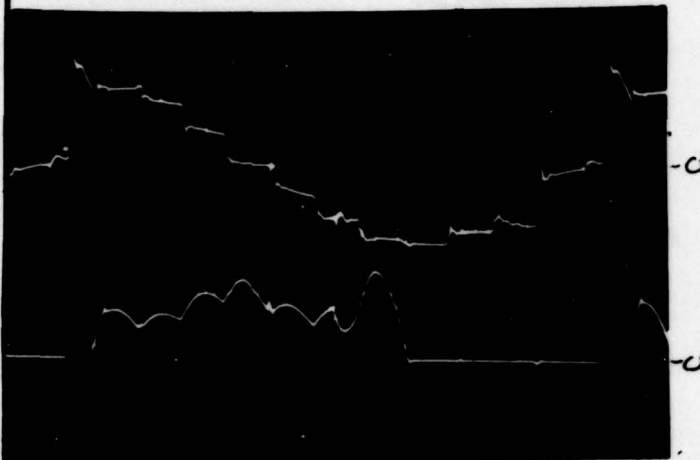
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STEP VOLTAGES AND CURRENTS - 400HZ, THREE PHASE



PC 3 2 1 0 1 2 3

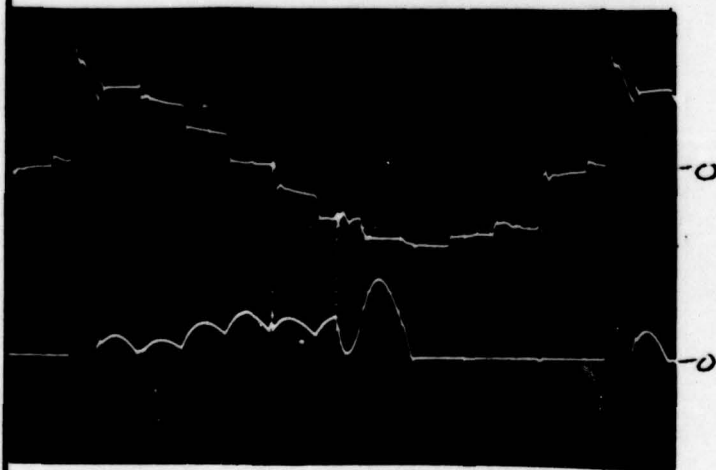
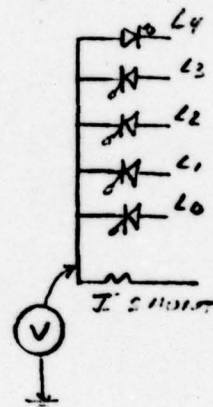
LEFT SIDE STEP  
VOLTAGE

100V/DIV.

NO LOAD

STEP CURRENT

100A/DIV. 100μSEC/DIV.



11KW, PF=0.8

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ITEM NO.

0009

PAGE

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DATA

PAGE

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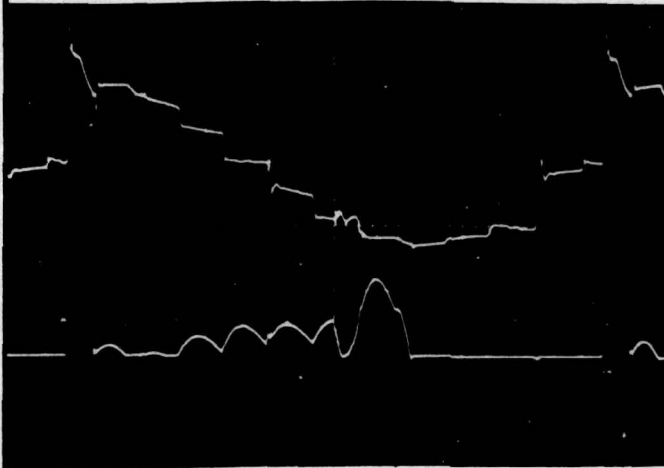
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CORRY 5/8/75

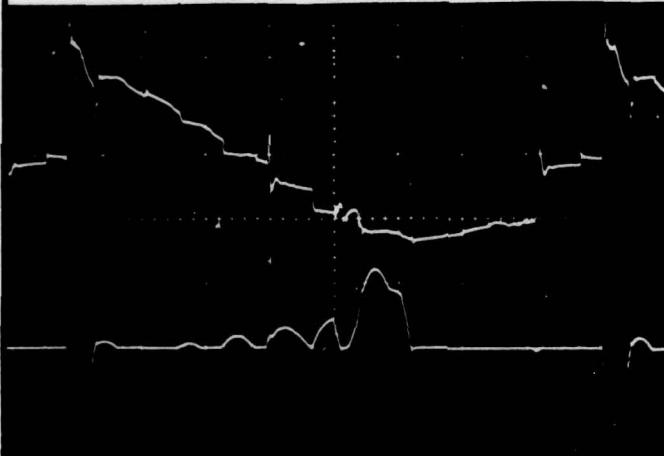
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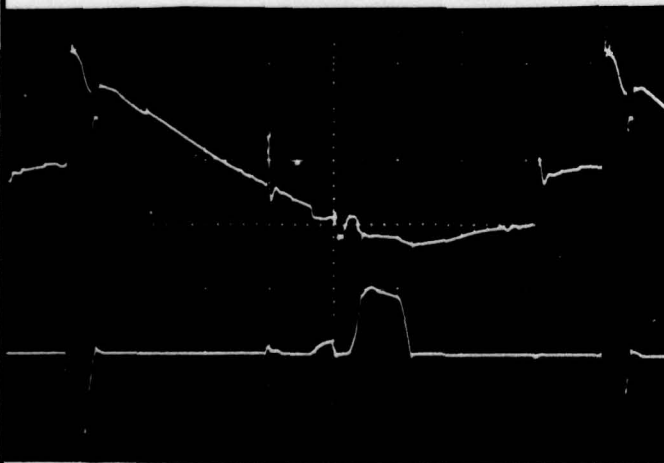
APPROVED



16KW, PF=0.8



20.6KW, PF=0.8



24.8KW, PF=0.8

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ITEM NO.

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PAGE

JOB NO.

DESIGN

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PAGE

84

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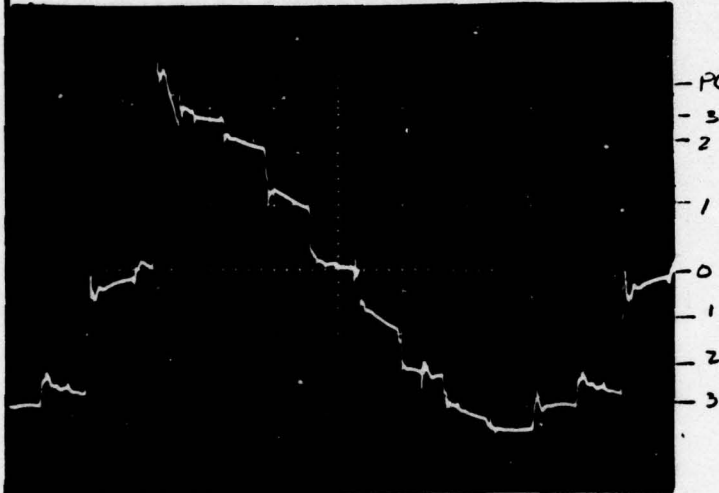
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APPROVED

AUTOTRANSFORMER STEP VOLTAGES 400HZ, THREE PHASE

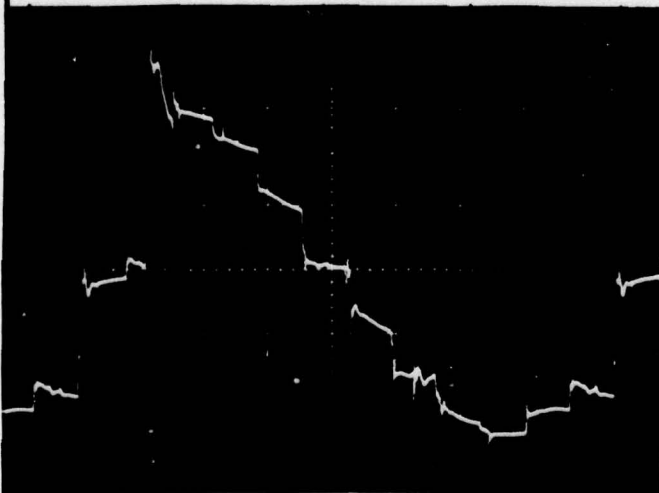


Y STEP FUNCTION

NO LOAD

50V/DIV.

100μSEC/DIV.



11KW, PF=0.8

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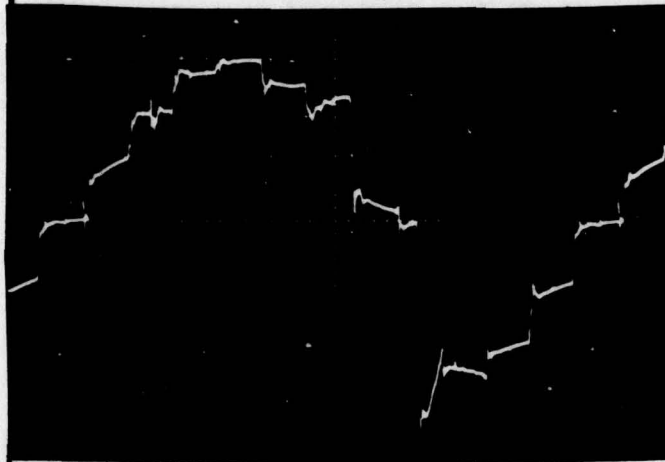
CORRY

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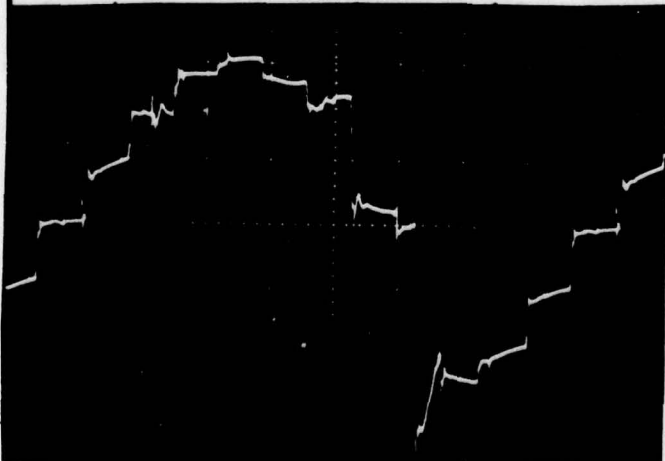


X STEP FUNCTION

NO LOAD

50V/DIV.

100μSEC/DIV.



11KW, PF=0.8

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REPORT NO.

ITEM NO.

0009

PAGE

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DESIGN

DATA

PAGE

86

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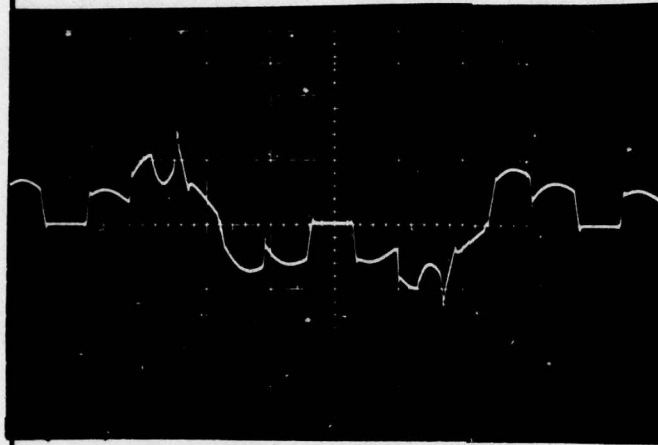
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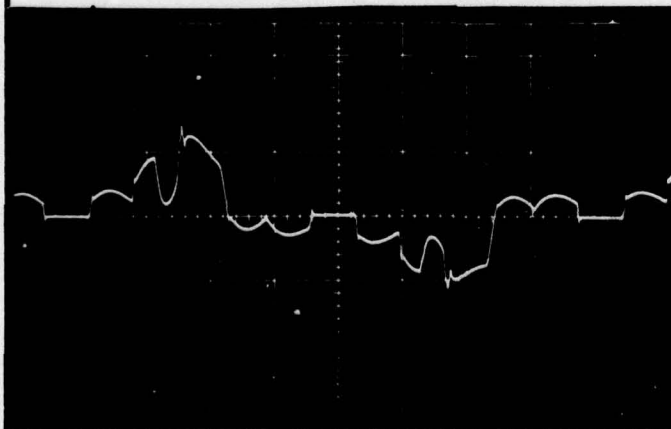
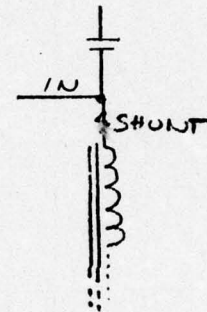
APPROVED

STEP TRANSFORMER CURRENT 400HZ, THREE PHASE



NO LOAD

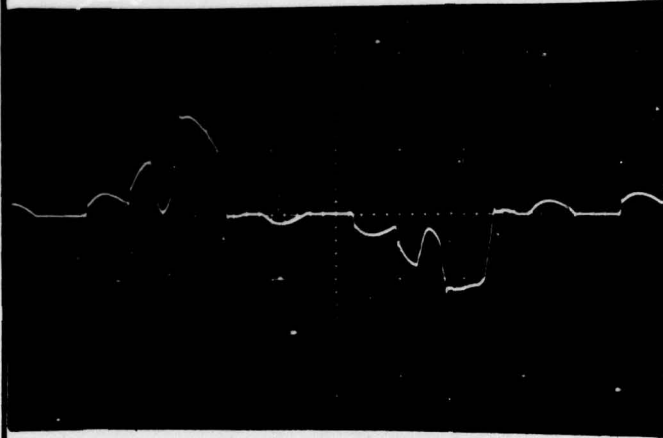
50A / DIV.



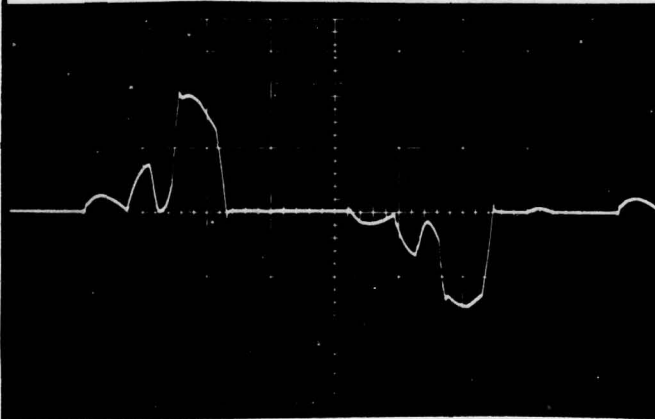
11KW, PF=0.8

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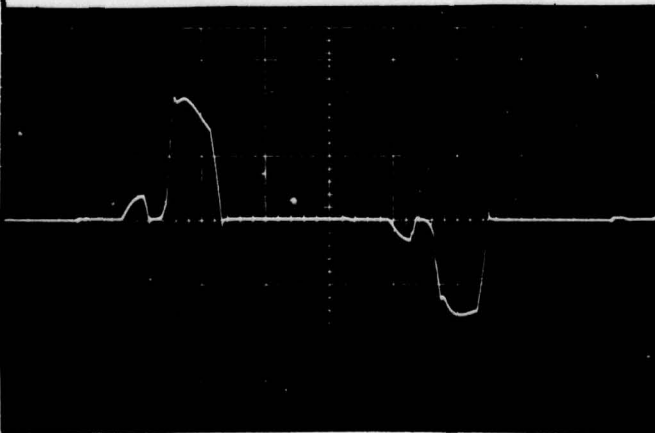
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	TITLE		
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16KW, PF=0.8



20.6KW, PF=0.8

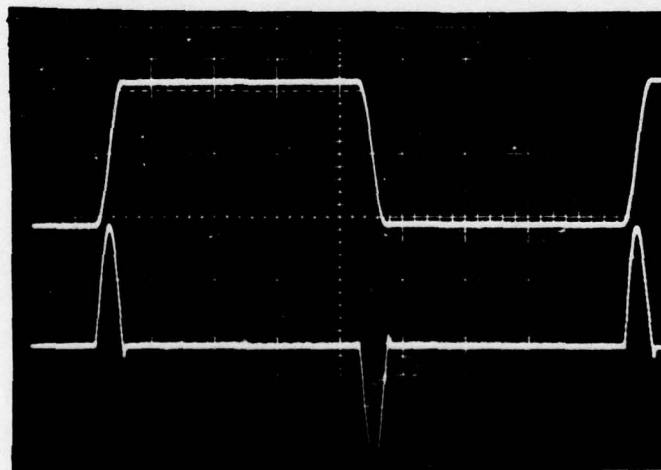
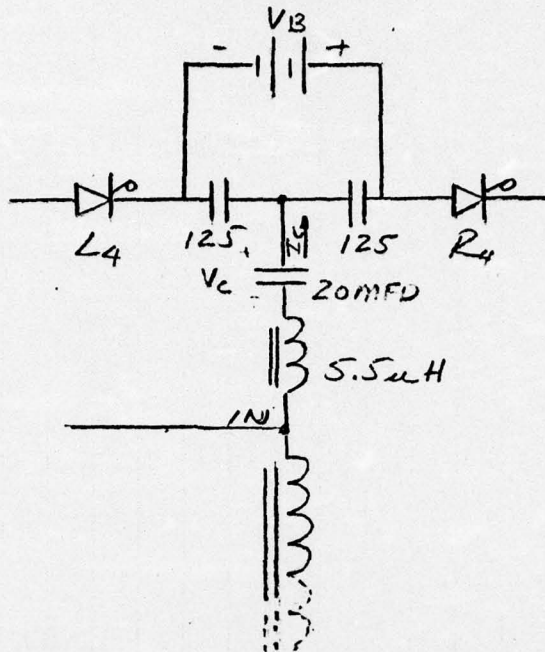


24.8, PF=0.8

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	TITLE		DATE 5/8/75
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# 400 HZ POWER CENTER COMMUTATION



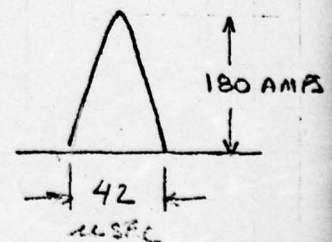
$V_B = 70 \text{ VDC}$   
 $I_B = 5 \text{ AMPS}$

$V_C \quad 100 \text{ V/DIV}$

$I_C \quad 100 \text{ A/DIV.}$

$V_{C \text{ RMS}} = 113.5 \text{ V RMS}$

$I_{C \text{ RMS}} = 41.5 \text{ A RMS.}$

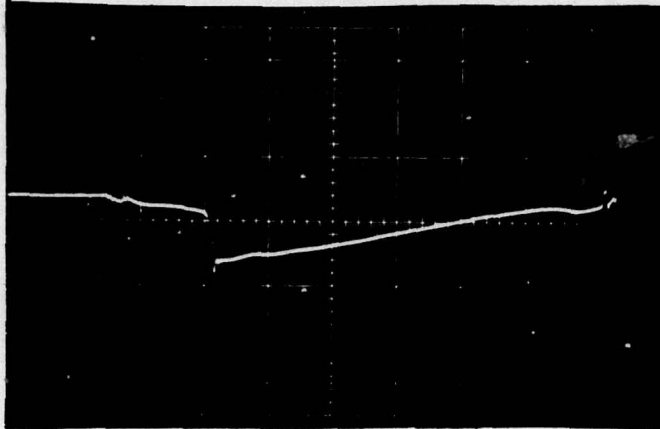


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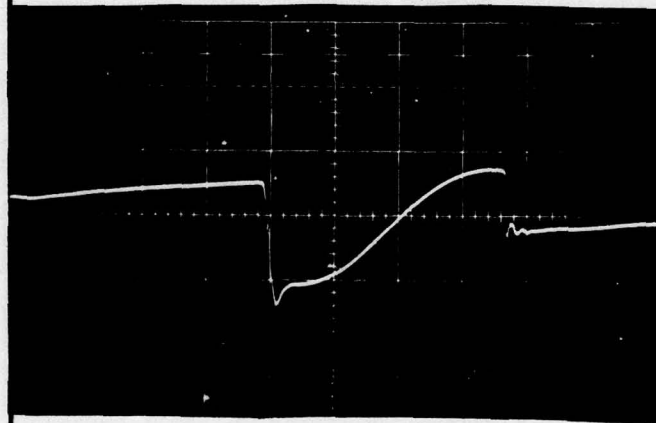
REVERSE BIAS TURN-OFF TIMES 400HZ, THREE PHASE



POWER CENTER  
P<sub>1</sub> TURN-OFF

5V/DIV.  
5μSEC/DIV.

20.6KW, PF=0.8



T- TURN-OFF

20V/DIV.  
5μSEC/DIV.



R<sub>3</sub> TURN-OFF AS R<sub>2</sub> TURN-ON

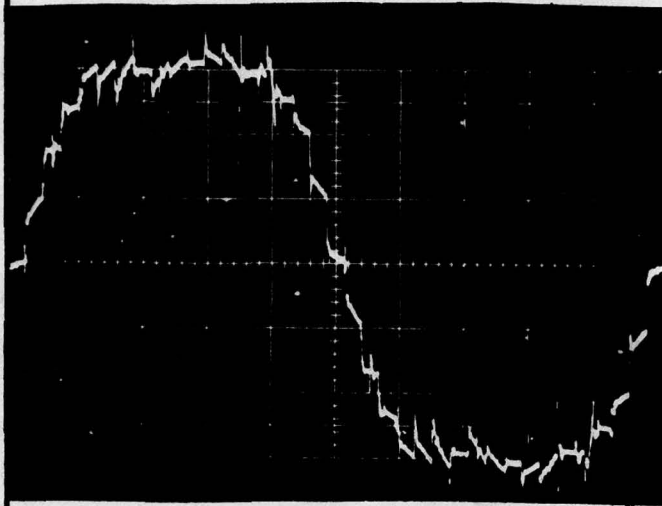
50V/DIV.  
50μSEC/DIV.

R<sub>3</sub> GATE

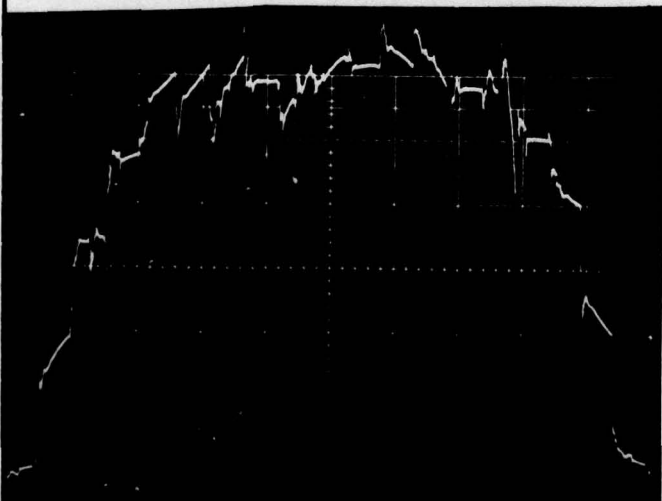
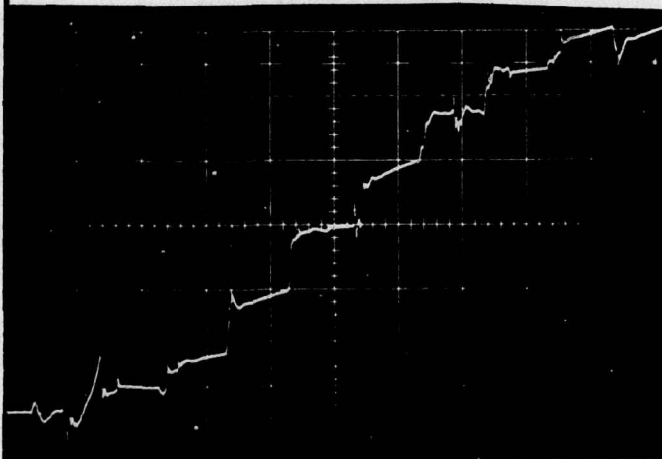
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	0009		DATA	90
TITLE		PREPARED	DATE	
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		CHECKED		
		APPROVED		

INVERTER BASIC VOLTAGES 400HZ NO LOAD



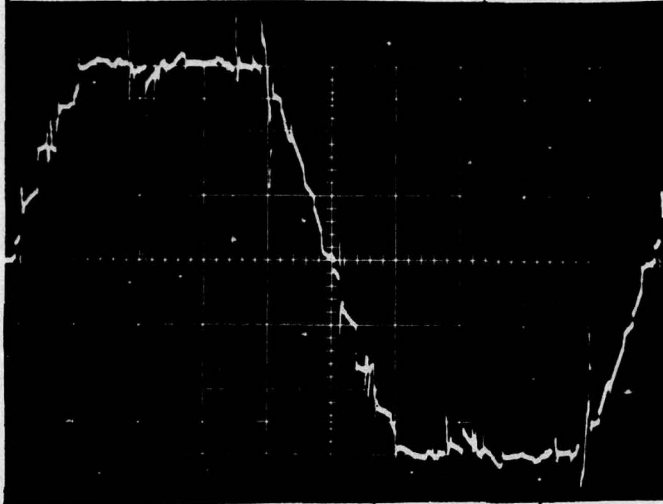
$V_{c-n}$



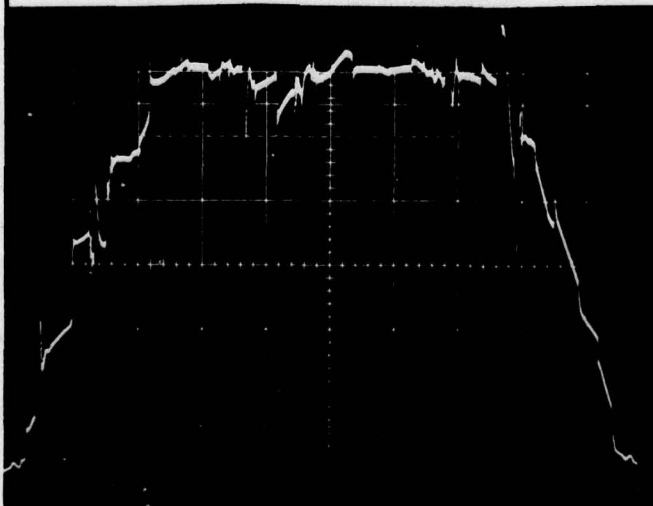
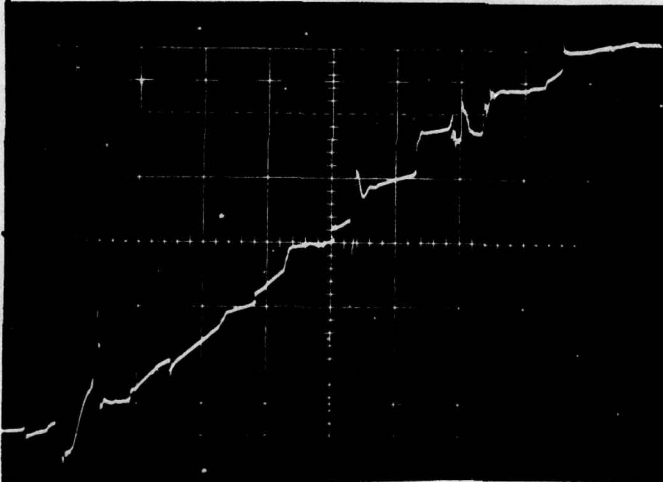
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	TITLE		
PREPARED CORY		DATE 5/8/75	
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INVERTER BASIC VOLTAGES 400Hz 20.6KW, PF=0.8



Vc-n



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GENERAL MOTORS CORPORATION

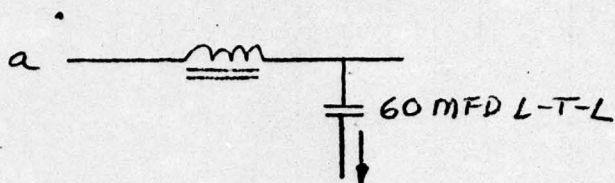
REPORT NO.  
ITEM NO.  
0009

PAGE JOB NO.  
DESIGN  
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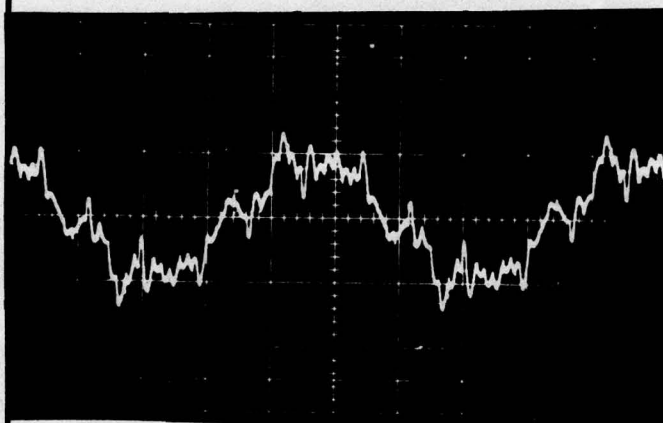
PAGE  
92

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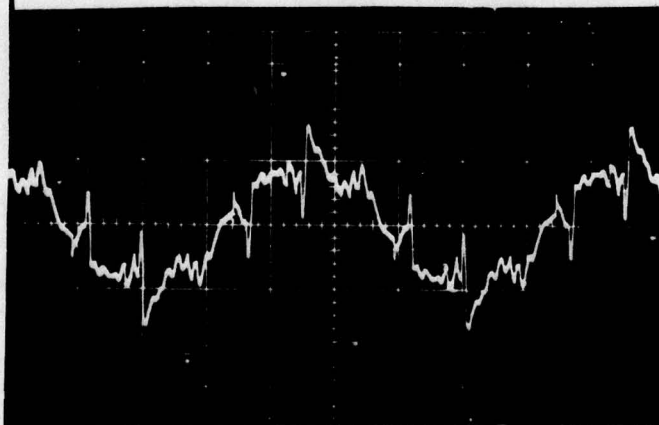
CURRENT THRU 60 MFD. CAPACITOR, 400 HZ



NO LOAD

50A/DIV.

500 μSEC/DIV.



20.6 KW, PF=0.8

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APPENDIX A

U. S. ARMY MOBILITY EQUIPMENT RESEARCH AND DEVELOPMENT CENTER  
FORT BELVOIR, VIRGINIA

PURCHASE DESCRIPTION  
FOR  
GENERATOR SET, ELECTRIC, TRANSPORTABLE, GAS TURBINE ENGINE DRIVEN  
SKID MOUNTED, ALTERNATING CURRENT  
MULTIFREQUENCY, 100 KW

1 June 1970

1. SCOPE - This purchase description covers a turbo-alternator type of gas turbine engine driven generator set to be used for supplying alternating current for military ground power applications.

1.1 Classification - The generator set shall be rated .100 KW, 0.8 power factor lagging, 3 phase, 4 wire, and connectable for the following output voltages and frequencies:

- a. 208 volts line-to-line and 120 volts line-to-neutral at 60 hertz (Hz).
- b. 416 volts line-to-line and 240 volts line-to-neutral at 60 Hz.
- c. 208 volts line-to-line and 120 volts line-to-neutral at 400 Hz.
- d. 416 volts line-to-line and 240 volts line-to-neutral at 400 Hz.
- e. 208 volts line-to-line and 120 volts line-to-neutral at 50 Hz.
- f. 416 volts line-to-line and 240 volts line-to-neutral at 50 Hz.

Z34.10 - Octave-Bank Filter Set for Analysis of Noise and Other Sounds, Specifications For

(Applications for copies should be addressed to the American Standards Assoc. 10 East 48th St., New York, New York)

3. REQUIREMENTS

3.1 Description - The generator set shall consist of a gas turbine engine directly coupled to a high speed, solid rotor, brushless alternator, a frequency converter and all supporting equipment, systems, and devices required to achieve a complete operable engine generator set (herein after referred to as "generator set") which will comply with all requirements of this purchase description. The generator set shall be designed for low cost of manufacture, and simplicity of operation and maintenance by personnel having a minimum of training.

3.2 Overall Generator Set Design - The overall generator set shall be designed with a systems concept but shall retain practical interfaces between components to facilitate procurement from multiple sources, standardization with other systems, and easy replacement of components. Hardware design should be consistent throughout the generator set in degree of sophistication, reliability, and emphasis on size and weight. The generator set shall be designed and constructed to withstand the extremely hard usage encountered in military service, including transportation and extreme environmental conditions. The generator set design shall emphasize simplicity and low cost with a selling price goal of \$25,000 or less per unit (in quantities of 200 units).

3.2.1 Power Rating - The generator set shall provide a net continuous electrical power output at the generator set output terminals of 100 KW, 0.8 PF lagging, at all voltages and frequencies of paragraph 3.5.1.1, at all environmental conditions of paragraph 3.2.10.1, when using fuels of paragraph 3.2.11, for the operating life of paragraph 3.2.7.

3.2.2 Size - The design goal shall be minimum overall dimensions consistent with other design requirements, with length, width, and height proportions suitable for easy transportation by rail, truck, trailer, or airplane.

3.2.3 Weight - The overall allowable dry weight for the generator set shall not exceed 1800 lbs with a goal of 1500 lbs. maximum. (See 6.4.9)

3.4.13 Waveform - In addition to being compatible with the input requirements of the static frequency converter (see 3.5), the alternator output waveform shall not contain any notches or spikes that could falsely trigger logic or thyrister circuitry within the converter. Harmonic content shall be kept to a low value to minimize alternator losses.

3.4.14 Efficiency - The efficiency of the combination alternator, voltage regulator and frequency converter (see 3.5) shall not be less than 85 percent for rated output at any rated voltage and frequency.

3.5 Frequency Converter - The frequency converter shall be a static, solid state, cycloconverter type, modular in construction and easily removable from the generator set. Use of electronic tubes shall not be permitted. Circuitry within the module(s) shall be arranged for ease of systematic trouble shooting. All circuit boards shall be marked as to function and the associated output phase relationship as applicable and shall be keyed to prevent exchanging or reversing of the circuit boards. SCR's shall be grouped and marked according to the associated output phase. The combination converter and alternator shall be capable of operating satisfactorily and controlling the output voltage as specified herein, through the range of voltages specified in 3.5.1.1. Voltage "build-up" in the combination converter and alternator shall be automatic and shall not require the use of any manual flashing circuits. Use of separate fans or blowers for forced cooling is not preferred. The converter module(s) shall be fitted with removable protective covers as necessary. Output power connections shall be made through conspicuously marked terminals. The terminals shall be rigidly mounted and shall not twist or turn in their mountings when the nuts are tightened. Connections to and from the module(s) for signal and DC control wires shall use a MS connector(s) in accordance with MIL-C-5015. No terminal blocks or solder connections shall be permitted for such signal and DC control wires.

-3.5.1 Voltage Requirements - The converter, together with the alternator and the control circuitry, shall perform as follows:

3.5.1.1

Voltage Operating Range - The generator set shall operate, within the requirements of this specification at any load from no load to rated load at any power factor from unity to 0.8 lagging at any rated frequency, at any voltage between 92 and 115 percent of rated voltage. (See 1.1)

3.5.1.2

Voltage Adjustment - By means of a manual rheostat on the control cubicle, it shall be possible to adjust the voltage to any value between the limits as stated in 3.5.1.1 at any load up to and including rated load at any power factor from unity to 0.8 lagging at any ambient temperature within the specified temperature range and at any rated frequency.

3.5.1.3

Voltage Waveform - With the converter operating at any load from no load to rated load at any power factor between unity and 0.8 lagging at any rated frequency, the following requirements shall apply to the line-to-neutral and line-to-line voltage waveforms:

- a. The deviation factor shall not exceed five percent.
- b. No single harmonic shall exceed two percent of the fundamental.
- c. Total harmonic content (square root of the sum of the squared values of all the harmonics) shall not exceed five percent of the fundamental.
- d. The DC voltage component as measured at the output terminals shall not exceed 100 millivolts.
- e. There shall be no evident discontinuities, spikes or notches in the waveform when viewed on a high frequency oscilloscope having a minimum display area of 6 cm by 10 cm, DC to 15 MHz (or greater) bandwidth and 23 nanoseconds (or less) risetime. To observe the waveform, the oscilloscope vertical gain shall be set such that the visible full screen portion of the trace is less than one tenth of the peak-to-peak voltage amplitude and the oscilloscope time base set such that the visible full screen portion of the trace is less than one tenth of the period of the voltage wave. By using the oscilloscope position controls, each portion of the wave shall be carefully examined.

The above requirements are based on use of linear (non-saturating) reactors to obtain the lagging power factor load component.

3.5.1.4

Phase Voltage Balance - With the generator set operating at rated output voltage, frequency, and no load, the maximum difference in the three line-to-neutral and line-to-line voltages as measured at the output terminals shall not exceed one percent of the rated line-to-neutral or line-to-line voltage respectively.

3.5.1.5

Phase Angle Balance - With the generator set operating at rated output voltage, frequency and at any load from no load up to and including rated load the angle between any adjacent output voltage vectors shall not differ from 120 degrees by more than one degree.

3.5.1.6

Effect of Unbalanced Load - With the generator set operating at no load, rated voltage and frequency, application of a single phase, line-to-line, unity power factor load equal to 25 percent of rated current shall not cause the three steady state line-to-line voltages to differ from each other by more than five percent of rated voltage.

3.5.1.7

Voltage Modulation - When viewed on the oscilloscope specified in 3.5.1.3, the output voltage envelope of any line-to-line or line-to-neutral voltage for any load up to and including rated load on the generator set shall not show a difference in the voltages of adjacent peaks of more than 1.5 volts. This requirement shall apply for both the upper and lower halves of the envelope. There shall also not be any repetitive pattern of the voltage peaks with a frequency less than one half rated output frequency.

3.5.1.8

Voltage Regulation - The voltage regulation from no load to any load up to and including rated load, and from any load up to and including rated load to no load shall not be more than one percent of the rated voltage (see 6.4.11).

3.5.1.9

Voltage Variation at Constant Load - At any constant load between no load and rated load, the generator set output voltage shall not deviate more than one half of one percent from its average rms value. There shall be no sustained periodic voltage oscillations, sustained periodic voltage oscillations, even though within the allowable one half percent variations at constant load; this requirement shall apply under all conditions, including those which exist after "settling" takes place following load changes as mentioned in 3.5 1.12b.

3.5.1.10

Long Term Voltage Stability (4 Hours) - At constant ambient temperature, constant barometric pressure, constant output frequency, constant voltage setting and at any constant load from no load to rated load, the output voltage shall remain within a bandwidth of two percent of rated voltage.

3.5.1.11

Voltage Drift - With the generator set operating at constant load and frequency, a change in ambient temperature up to 60°F in an eight hour period (generator set temperature stabilization being accomplished at both the initial and final ambient temperature conditions) or as the generator set stabilizes from cold conditions at any load, shall not cause the voltage to change by more than one percent of rated voltage.

3.5.1.12

Transient Voltage Performance - Performance (as measured by a light-beam oscillograph) of the generator set during the following specified transient conditions shall be as follows:

a. With the generator set initially operating at no load, rated voltage and rated frequency, the rms terminal voltage of the generator set shall not drop to less than 75 percent of rated voltage when a balanced, 3 phase, low power factor (0.4 pf to 0.2 pf, lagging), static load having an impedance of 0.5 per unit (drawing twice rated current at rated voltage) is suddenly applied to the output terminals of the generator set. When connected to the specified load, the generator set shall recover to a minimum of 95 percent rated voltage within 0.7 seconds and shall stabilize at or above this voltage. The above specified voltage dip shall not be exceeded when a fully-loaded induction motor of the above specified impedance is used in place of a static load, and no reactions shall be set up to prevent full acceleration of the motor with rated torque applied to its shaft.

b. When the generator set is initially operating at rated frequency, rated voltage and following any sudden change in load from no load to rated load, the instantaneous rms voltage shall not drop to less than 88 percent of rated voltage and shall reach stable conditions (as defined in 6.4.12) within 0.5 second; no overshoot or undershoot (see 6.4.13) of the final voltage may exceed the initial voltage transient in amplitude. The above requirements shall also apply when load is suddenly changed from rated load to no load, except that the initial voltage transient shall involve a voltage rise not to exceed 115 percent of rated voltage.

c. The generator set shall be capable of across-the-line starting a motor rated at 0.5 horsepower per KW of generator set rating. The starting current rating of the motor shall be NEMA code F and the motor shall be loaded with a flywheel having an inertia equal to that of the motor. Satisfactory starting is defined as acceleration of the motor to rated speed without tripping any safety device.

3.5.1.13

Short Circuit - The generator set shall withstand without injury, application of any ten second short circuit (3 phase, single phase L-L, and single phase L-N) at the generator set output when operating at rated kilowatts, power factor, frequency, and voltage. During the application of the short circuit, the sustained steady state short circuit current shall not be less than 250 percent of rated current (see para. 6.4.19) for the duration of the short.

3.5.2

Frequency Requirements - The frequency reference circuit shall be capable of attaining and maintaining the required converter output frequency as soon as the alternator output voltage is applied to the converter. This shall be accomplished by using temperature compensation circuitry as necessary. Output of the circuit shall provide the required three-phase signals to synchronize the converter phases and maintain the phase relationship as required in 3.5.1.5. The frequency circuitry shall be capable of driving or synchronizing up to two additional, identical, generator sets operating in parallel. This shall be accomplished through a paralleling receptacle.

3.5.2.1

Frequency Operating Range - The operating frequencies shall be 50, 60 and 400 Hz and the generator set shall be designed to meet operating requirements of paragraphs 3.5.2.2, 3.5.2.3, and 3.5.2.4 without adjustment. Manual trim of the output frequency shall not be required for any mode of operation when the generator is connected for 50, 60, or 400 Hz.

3.5.2.2

Frequency Regulation - The generator set shall provide isochronous operation within 0.1%, i.e., for every load change up to and including rated load the frequency regulation (see 6.4.11) shall not exceed  $\pm 0.1\%$ .

3.5.2.3

Long Term Frequency Stability - The generator set frequency shall not vary more than 0.05% of the rated frequency during any four-hour period of operation over the range of environmental requirements of this specification at any constant load from no load to rated load.

3.5.2.4

Transient Frequency Performance - For application or removal of any load up to and including rated load the frequency of the generator set shall not change during the load transient by more than  $\frac{1}{4}$  of one percent of rated frequency and shall return to the original operating frequency within 0.1 seconds (see 3.5.2.2).

3.5.2.5

Frequency Modulation - When viewed on the oscilloscope specified in 3.5.1.3, the output voltage for any load up to and including rated load on the generator set shall have a zero crossover that does not fluctuate by more than plus or minus one half percent of the period of the output voltage wave. This requirement shall apply to both the positive and negative going portion of the voltage wave. There shall also be no sustained periodic frequency oscillations of the output voltage fundamental frequency.

3.5.3

Parallel Operation

3.5.3.1

Load Division - The generator set shall be capable of isochronous parallel operation with two other identical generator sets. With their frequency and voltage regulator paralleling circuits properly interconnected, any two sets of the same rating operated in parallel shall divide load in accordance with the following as system load at rated power factor is varied between zero and 100 percent (and vice versa) of the combined rating of the connected sets:

- a. Real Power Division - At no time shall the difference between the steady state kilowatt outputs of the sets be greater than ten percent of the kilowatt rating of one set.
- b. Real Power Exchange - At any constant system load up to the combined rating of the sets in parallel, real power exchange between the sets shall not exceed ten percent of the kilowatt rating of one set. Real power exchange is the difference between the maximum and minimum instantaneous real power output delivered by one set, for constant system load conditions, as determined from oscillographic measurements.

- c. Reactive Power Division - At no time shall the difference between the average reactive KVA outputs of the sets be greater than ten percent of the KVA rating of one set.
- d. Reactive Power Exchange - An any constant system load up to the combined rating of the sets in parallel, reactive power exchange between the sets shall not exceed ten percent of the KVA rating of one set. Reactive power exchange is the difference between the maximum and minimum instantaneous reactive power output delivered by one set, for constant system load conditions, as determined by oscillographic measurements.

For the above requirements, the initial system load shall be equally divided between the sets, both as to active and reactive components; thereafter, there shall be no adjustments to frequency circuits, voltage regulators, or any other component as system load is changed. These requirements shall also apply when three sets are connected in parallel.

3.5.3.2 Automatic Synchronization - With identical generator sets interconnected with the paralleling cable, the automatic synchronization circuits shall be energized with the "unit-parallel" switches (see 3.6.2.10) are set for parallel operation. The circuits shall automatically synchronize both the frequency and voltage of the generator sets to be paralleled. This circuit shall not interfere with normal operation of the generator sets when the paralleling cable is disconnected and/or the "unit-parallel" switch is actuated from either the "unit" position to the "parallel" position or vice versa.

3.5.3.3 Improper Paralleling Procedure - The generator sets shall not be damaged in the event generator sets are connected in parallel with their output voltages being out of phase up to and including 180 degrees, with the "unit-parallel" switch in the unit or parallel position.

3.6 Control Cubicle - A control cubicle shall be mounted at the alternator end of the generator set. Ventilation of the control cubicle shall be provided as necessary to prevent buildup of high temperatures within the cubicle. The control cubicle shall contain all controls, switches, instruments, etc., necessary to start, operate and monitor the set. It may also contain relays and control devices not suitable for

APPENDIX B

# A STEP FORMING CIRCUIT FOR SINE WAVE INVERTERS

Thomas M. Corry

Delco Electronics Division  
General Motors Corporation  
Santa Barbara, California

Razi A. Kokan

Robert A. Williams

United States Army  
Ft. Belvoir, Virginia  
Mobility Equipment R&D Center (MERDC)

## ABSTRACT

This paper considers three aspects in the optimum design of 15 to 100 kVA, 60 Hz three-phase inverters: thyristor commutation, voltage waveform design, and component selection. The first aspect is the method devised for commutating thyristors in obtaining the stepped voltages used to shape the inverter output voltages. Requirements of the commutation circuit are discussed and the step circuit operation is described. The second aspect is computer implementation of procedures for designing voltage waveforms to minimize inverter cost, weight, and volume. An illustration is provided of N-step voltage waveform design to minimize total harmonic distortion, or logic circuit costs; to maximize power handled by the power center thyristors; or to reduce magnitudes of the 5th and 7th harmonics. The third aspect considered is how inverter weight, volume and cost are affected by total harmonic distortion of the inverter unfiltered output voltages. Results of a design study were plotted to show how the relative cost, volume and weight of the THD-dependent components vary with the number of voltage taps used on the step transformer.

## INTRODUCTION

In a program sponsored by the United States Army Mobility Equipment Research and Development Center (MERDC), Delco Electronics developed a general purpose inverter capable of producing 15 kVA, 60 Hz or 400 Hz, three phase power or 10 kVA, two-wire or three-wire, single phase power from either dc or rectified ac power sources. Continued development, as reported in this paper, has resulted in a step voltage circuit for the MERDC inverter, a computer programming procedure for waveform design, and a design optimization approach for a 100 kVA, 60 Hz inverter.

The 15 kVA inverter<sup>1</sup> generates stepped waveform approximations of sine waves by varying the voltage levels on a tapped autotransformer. The required step changes are obtained with a special commutation circuit supplied with constant commutation energy independent of inverter input voltage, magnitude of the voltage step, or inverter load current. To effectively transfer this energy to the commutation loop, an energy source circuit is operated in synchronism with the thyristor turn-off circuit. The constant energy commutation capability allows the inverter to function with greater than two per unit short circuit currents and to start up with full load.

The step wave circuitry and waveform design techniques described herein are being used to develop candidate inverter systems for U.S. Army general purpose power conditioners. These units rated between 15 kVA and 100 kVA, will produce precision three-phase power, at 60 Hz or 400 Hz, in conformance with MIL-STD-1332B, Class I. The inverters will be usable in turbo-alternators, diesel generator sets, utility line upgrading, and frequency converters.

<sup>1</sup> T.M. Corry. "A New Concept for Generating Three-Phase Sine Wave Voltages with Semiconductor Power Switches." 1973 PESC. Record pages 230-236, 73 CHO 863-1 AES.

## STEP VOLTAGE COMMUTATION

Figure 1 shows the power circuit organization of the general purpose inverter and the waveform it produces. The power center thyristors generate the flat topped voltage portion of the line-to-neutral waveform, during which 60 to 80% of the three phase power flows into the load. As thyristors T<sup>+</sup>, T<sup>-</sup> excite the step transformer at a frequency three times the output frequency of the inverter, step voltages are generated (as two sets of stair-stepped voltages) and are distributed to the three-phase output lines via phase selectors. Thus, the width of the flat topped voltage wave and the number of voltage taps on the step transformer determine the total harmonic distortion (THD) of the unfiltered output voltage.

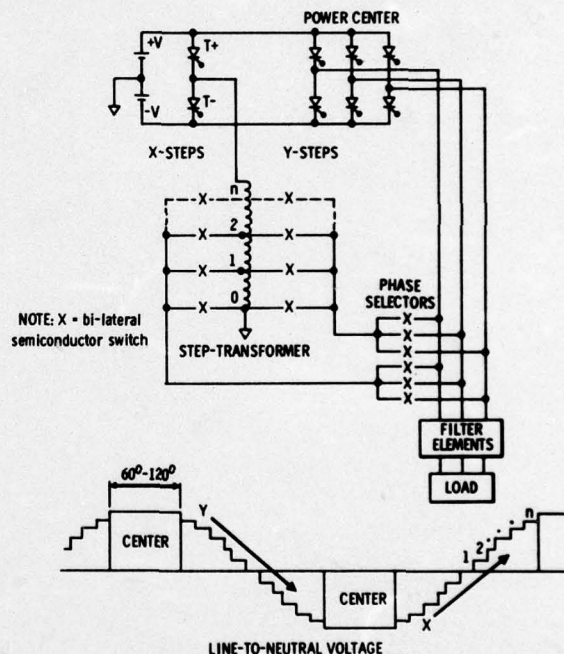


Figure 1. Inverter Circuit Concept and Line-to-Neutral Voltage

The general waveform<sup>2</sup> of the inverter line-to-neutral voltage is considered to be made up of three functions: center function, Y function and X function. In waveform optimization studies, the center function was varied over a range of 60° to 120° and the number of voltage steps (counted from the zero reference) ranged from one to ten. The Y and X voltage function producing circuits (shown in Figure 2) use thyristors to change voltage taps on the step generating autotransformer. The thyristors in the Y and X function cir-

<sup>2</sup> U.S. Patent No. 3,725,767

cuits are divided into two ladders, one self-commutated and the other requiring an auxiliary commutation circuit.

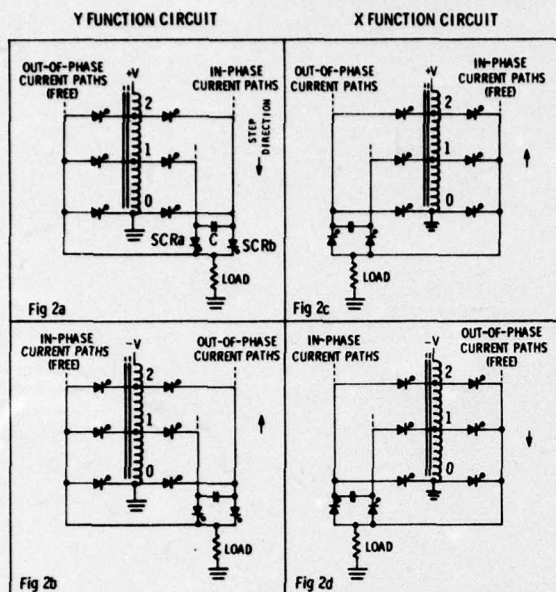


Figure 2. Y and X Step Function Circuits

In the Y function circuit (Figure 2a) out-of-phase currents flow through the self-commutated thyristor ladder (on the left). When a positive voltage is applied to the step transformer, the left hand thyristors are turned off as the voltage steps move down from the top step to the bottom. In-phase currents flow through the right side thyristors, which are turned off by the double bus commutation circuit consisting of thyristors SCRa, SCRb and capacitor C. When a negative voltage is applied to the step transformer (Figure 2b) in-phase currents flow on the left side and out-of-phase currents flow through the right side thyristors and commutation circuit. The X function circuit (Figures 2c and 2d) is an inverse image of the Y function circuit. Delco has fabricated test step circuits and successfully commutated currents representative of a 100 kW rating, using readily available components.

To aid in discussing double bus commutation<sup>3</sup>, Figure 3 provides a schematic of the Y and X function step circuits with the self-commutating thyristors not shown. Assume in Figure 3 that thyristors SCR2 and SCRb are conducting current to the Y function load, transformer polarity is positive, and capacitor C is charged as indicated. To transfer the load current to voltage level 1, SCRa is gated on 35  $\mu$ s prior to SCR1. The discharge of capacitor C reverse biases SCRb and turns it off. SCR2 is turned off by the reverse voltage ringup of capacitor C, which is then charged at the proper voltage polarity for the next step level change to level 0. Load current continues to flow through SCR1 and SCRa.

The thyristor, reverse voltage step commutation circuit of Figure 3 is the basic mechanism for turning off the double bus step thyristors. Commutation capacitor energy sources are the step voltage taps of the autotransformer. Hence, commutation energy varies with 1) the dc voltage applied to the inverter, 2) the step voltage magnitude, and 3) the inverter load current.

When commutation energy is obtained only from the step transformer voltage, the inverter cannot operate with short circuit loads or start with large loads. To provide these capabilities, a commutation boost circuit was developed to hold the energy

stored in the commutation capacitor essentially constant and independent of inverter load or input voltage. The boost function re-

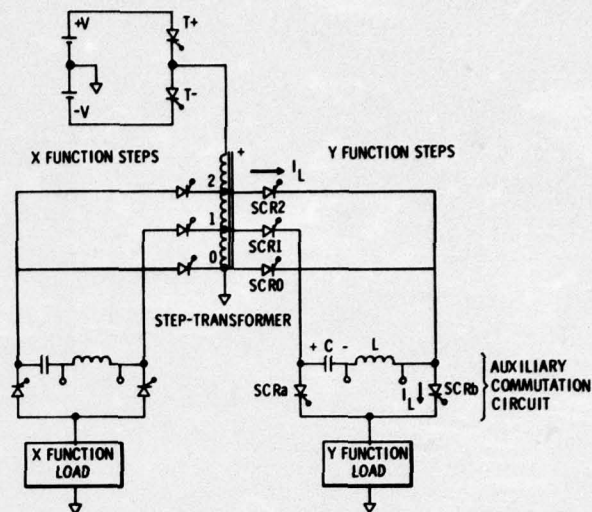


Figure 3. Double Bus Step Changing Circuits

quires a source of commutation voltage for each conducting step thyristor at the time voltage level changes. Figure 4 shows an alternating voltage energy source connected to the step commutation circuit of Figure 3. The commutation boost voltage energy source is a series resonant inverter operating in synchronism with the step commutation.

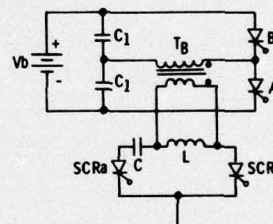


Figure 4. Boost Voltage Source for Step Commutation Circuit

The operation of the voltage boost circuit, in conjunction with the step commutation circuit, is depicted in Figure 5, which is an equivalent circuit of the boost circuit at the time that thyristor SCRB is being turned off. The current arrows shown are for con-

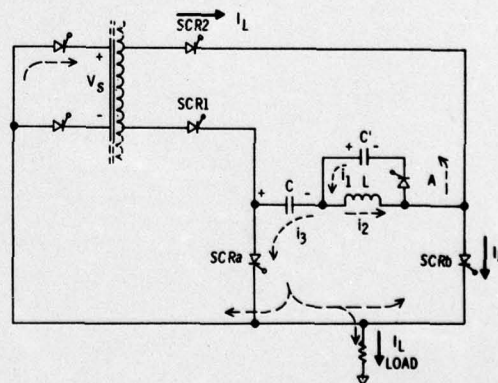


Figure 5. Boost Voltage Equivalent Circuit

ditions of load current being transferred from voltage step level 2 to step level 1, and current flow through thyristor SCR2 being transferred to thyristor SCR1. Thyristors SCRa and A are then

<sup>3</sup> T.M. Corry, R.M. McKechnie, R.A. Williams, "DC Link Inverter for Army Power Conditioner Requirements," 1974 PESC. Record pages 305-311. 74 CHO 863-1 AES.

turned on simultaneously, but 35 microseconds before the turn-on of thyristor SCR1. At the instant thyristors SCRa and A are turned on, the voltages of capacitors C and C' add. Energy stored in these capacitors is used to turn-off thyristor SCRb and supply load current and ringup current through thyristor SCR2. Note that the

step voltage  $V_s$ , between steps 1 and 2 of Figure 5, does not appear in the ringup circuit of capacitors C and C'. Therefore, the voltages across these capacitors are independent of the step transformer voltage, and are controlled by the boost voltage source  $V_b$  of Figure 4.

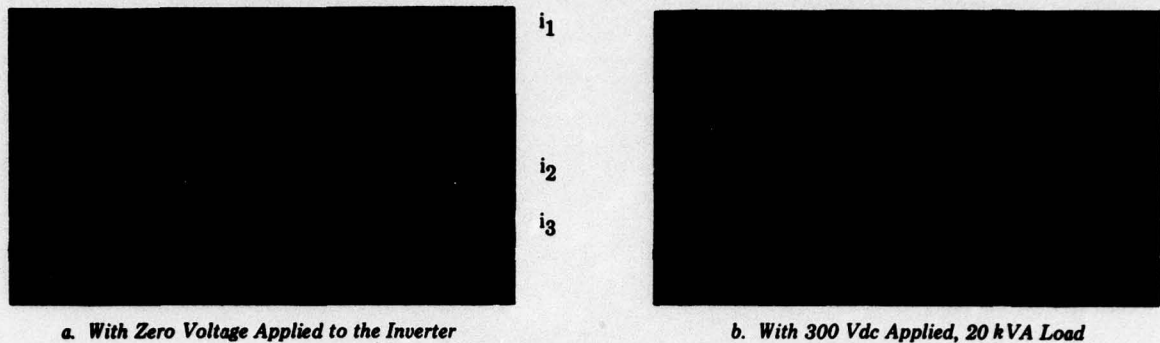


Figure 6. Commutation Circuit Currents

Figure 6 shows photographs of commutation currents  $i_1$ ,  $i_2$ ,  $i_3$  (of Figure 5) for two conditions: zero voltage applied to the inverter; and 300 Vdc applied, and with the inverter supplying a 20 kVA load. Note that the current magnitudes for the two conditions are virtually identical, indicating that commutation energy is independent of inverter input voltage or load.

A schematic diagram of a developed 15 kVA, 60 Hz inverter is shown in Figure 7. For this circuit, the voltage waveform was designed so that the Y and X function steps would switch in synchronism; this allows use of one voltage boost commutation circuit instead of two. The voltage waveform, having a  $110^\circ$ -wide power center and  $10^\circ$ -wide steps, is described in detail in Tables 1 and 2.

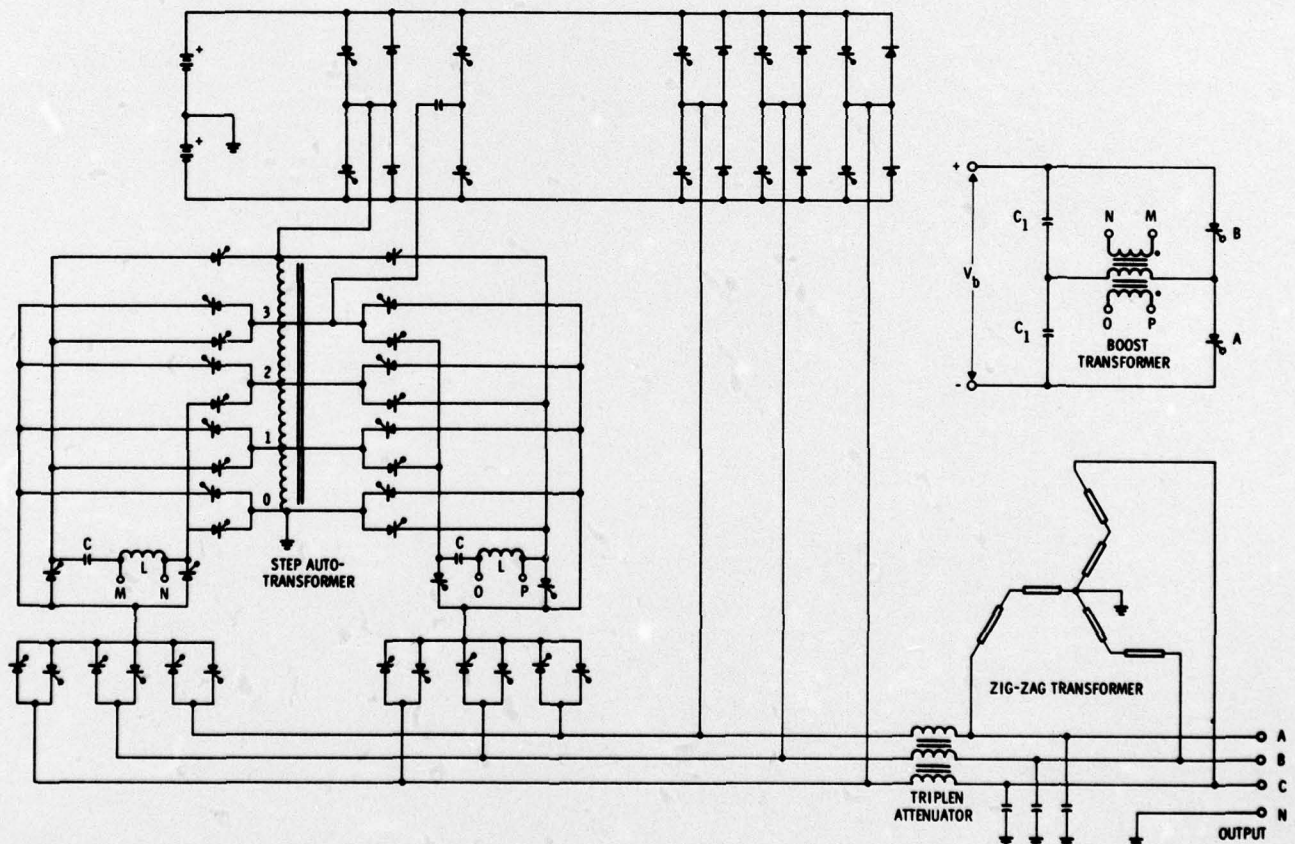


Figure 7. Schematic of 15 kVa, 60 Hz Inverter

## VOLTAGE WAVEFORM DESIGN

Waveform design is determined using a computer analysis program in order to minimize filtering and optimize hardware usage. Figure 8 shows the generalized form of the line-to-neutral voltage which the Delco inverter is capable of generating. The optimization problem is this: For  $N$  voltage steps, design a voltage waveform with the least possible total harmonic distortion by adjustment of step number, width and height. Since the third harmonic, and all multiples thereof, are eliminated by an attenuator in the inverter output circuit, (or are naturally absent) all triplen harmonics can be ignored in the optimization process. Various constraints can be added — such as equal-width voltage steps, minimum fifth and seventh harmonics, maximum-width power center, and number of voltage steps — which could reduce inverter logic cost and output filter size, maximize inverter efficiency, and minimize hardware cost.

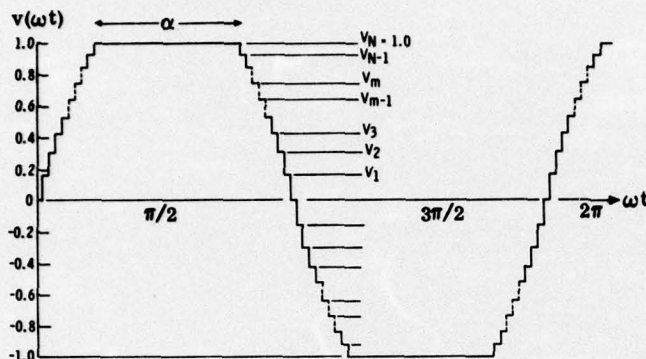


Figure 8. General Form of Line-to-Neutral Voltage

The numerical technique is to optimize one variable at a time and calculate the corresponding THD values. The value of the first variable yielding a minimum value of THD is chosen as the optimum value of the variable. Should there be more than one minimum value of THD when the variable is incremented, the value chosen is that which gives the lowest minimal THD. The optimization procedure is repeated for each remaining variable while holding the previously considered variables constant at their optimized values. Iterations are then repeated a preset number of times, or until the difference between minimum values of THD for two consecutive iterations is either zero or negligible.

A computer program (called OPTSWF)<sup>4</sup> was developed to implement the optimization for minimum THD. For each variable, the program applies three basic procedures: coarse optimization, averaging, and fine optimization. The input, assuming a constraint of equal step widths, can have any one of three forms:

- Form I — Value of the number of step levels  $N$ , initial values of the step width  $X$ , and  $N$  voltage step heights  $V_{1,0}, V_{2,1}, V_{3,2}, \dots, V_{N,N-1}$  are selected as input.
- Form II — Number of step levels  $N$  and width (in degrees) of the flat-top portion of the waveform are given. The program calculates initial values of step width  $X$  and voltage step heights are apportioned, assuming all step heights are equal. The program then enters the optimization of step width  $X$ .
- Form III — Desired value of step frequency harmonic is given. The program calculates the initial values of step width and the flat topped portion. Voltage step heights are given (as in Form I) and are computed assuming all heights equal (as in Form II).

<sup>4</sup> R.A. Kokan, "Method of Optimization for a Periodic Step Waveform for Minimum Total Harmonic Distortion." 1975 U.S. Army Numerical Analysis Conference (Feb. 11-12). U.S. Army Troop Support Command, St. Louis.

## VOLTAGE STEP WIDTH OPTIMIZATION

Although all step widths were assumed to be equal, varying the step width  $X$  will change the position of  $N$  step heights. This is equivalent to changing  $N$  variables simultaneously in equal steps. Since this will have the greatest impact on the THD function, step width  $X$  was chosen to be the first variable of optimization.

The initial value of step width  $X$  is input to the program along with four parameters for determining the variable "window" or range:

- XC = Coarse range parameter (fraction)
- XP = Coarse increment parameter (degrees)
- CT = Fine range parameter (degrees)
- PC = Fine increment parameter (degrees)

The coarse "window" is given by

$$(XC)(XINIT) \leq XOPT \leq (2-XC)(XINIT) \quad (1)$$

The fine "window" is given by

$$(XAVE-CT) \leq XOPT \leq (XAVE+CT) \quad (2)$$

### Coarse XOPT Procedure

The position of the "window" can be varied by changing the value of the initial step width  $XINIT$ . Its range can be varied by changing the value of  $XC$ . The limits on  $XC$  are

$$0.0 \leq XC \leq 1.0 \quad (3)$$

For convenience the first value of  $X$ , called  $X(1)$ , is rounded to the nearest degree or tenth of a degree depending upon the input value of a "FLAG"  $IXR$ . If  $IXR = 0$ , then  $X(1)$  is rounded to the nearest degree. If  $IXR = 1$ ,  $X(1)$  is rounded to the nearest tenth of a degree. The variable  $X$  is increased in increments finite from  $X(1)$  to  $X(K)$  in  $K$  steps within the window initially selected (Figure 9). The corresponding values of THD are calculated using the initial values of  $V_{m,m-1}$ . That value  $X(L)$  which gives the minimum value of THD in the coarse range  $THD(1)$  to  $THD(K)$  is the optimum value of  $X$ .

### Average XOPT Procedure

The value  $X(L)$  at which the THD ( $L$ ) was minimum is further refined by an averaging technique. The values of THD obtained at locations  $X(L-1)$  and  $X(L+1)$ , where the minimum THD is at  $X(L)$ , are compared in the following manner and the average optimum  $X$ , called  $XAVE$ , is obtained by

$$XAVE = \frac{X(L) + X(L+1)}{2} \quad \text{if } THD(L-1) > THD(L+1) \quad (4)$$

$$XAVE = \frac{X(L) + X(L-1)}{2} \quad \text{if } THD(L-1) \leq THD(L+1) \quad (5)$$

If the values of THD ( $K$ ) were varying, then for monotonically increasing values of THD ( $K$ )

$$XAVE = X(1) \quad (6)$$

and for monotonically decreasing values of THD ( $K$ )

$$XAVE = X(K) \quad (7)$$

### Fine XOPT Procedure

The fine optimizing procedure is similar to the coarse procedure, except that the fine increment  $PC < \text{coarse increment } XP$ , and the fine window is narrower than coarse window:  $CT < (1-XC)(XINIT)$ . In a manner similar to coarse tuning, the value of  $X$  is increased in increments of  $PC$  from  $X(1)$  to  $X(K)$  within the window defined by equation (2), and the corresponding values of THD are calculated. The optimum value of  $X(L)$  is that value of  $X$  giving the minimum value of THD.

Figures 9 and 10 show the optimization "window" of the variable X for a 4-step waveform. Figure 9 shows how THD varies with  $0.1^\circ$  incremental increases in step width X, inside the window ( $5.6^\circ$  to  $11.6^\circ$ ), as each of the four step heights is given its non-optimized value of 0.250. The THD changes from 10.8% to 5.58%. Figure 10 shows the window for the same variable when the four step heights have their optimized value of  $V_{1,0} = 0.332$ ,  $V_{2,1} = 0.277$ ,  $V_{3,2} = 0.199$  and  $V_{4,3} = 0.192$ . Note that the localized minima

in Figure 9 has been "fine-tuned" in Figure 10 by optimizing the step heights, and that the step width for optimum THD moved from  $8.2$  to  $10.8^\circ$  after step height optimization. The program was able to select the value of X ( $10.8^\circ$ ) which corresponds to a step frequency of the 33rd harmonic. That gives the lowest minimal value of THD (4.818%) at the optimum X. For the balance of the iteration, the step width is kept constant at its optimized value, XOPT.

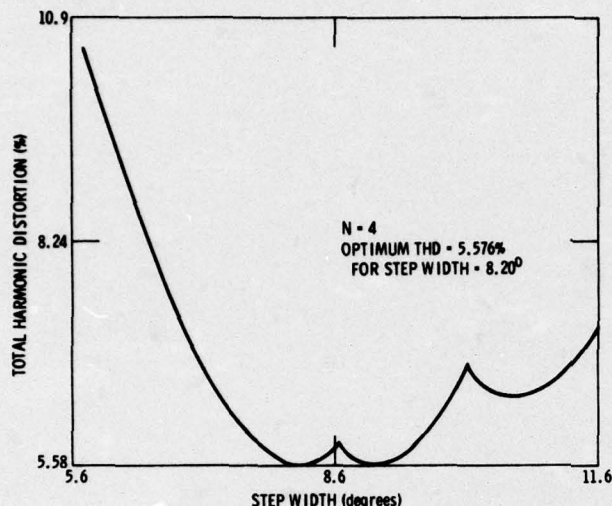


Figure 9. Effect of Step Width Variation on THD

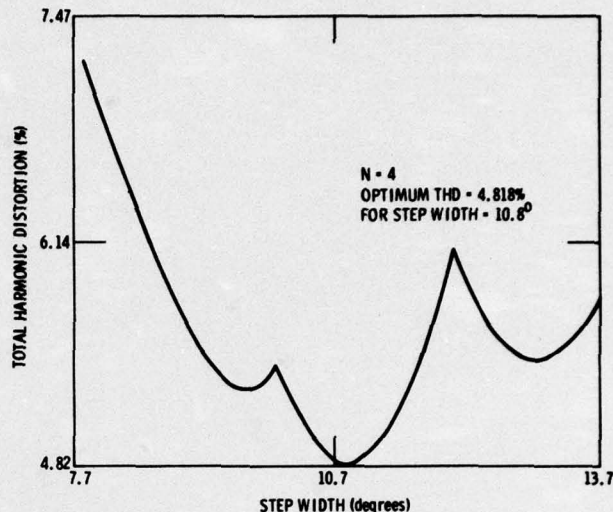


Figure 10. Effect of Step Width Variation with Step Heights Optimized

#### VOLTAGE STEP HEIGHT OPTIMIZATION

The N step heights are next optimized beginning with the bottom step height  $V_{1,0}$  and ending with the top step height  $V_{N,N-1}$ . All previous procedures for optimizing step width X are also used for step height. The following parameters (like those given for X) define the "window" for the step heights.

- VC = Coarse Range Parameter (fraction)
- VP = Coarse Increment Parameter (degrees)
- VCT = Fine Range Parameter (degrees)
- VPC = Fine Increment Parameter (degrees)

For each step height, the coarse window is

$$(VC) VINIT(m,m-1) \leq V_{m,m-1} \leq (2-VC) VINIT(m,m-1) \quad (8)$$

and the fine window is

$$VAVG(m,m-1) - VCT \leq V_{m,m-1} \leq VAVG(m,m-1) + VCT \quad (9)$$

where VC is a fractional constant between 0 and 1.0. The program assigns to each of the N step heights the initial value VINIT(m,m-1) at the start of optimization, for  $m = 1, 2, 3, \dots, N$ . These are given to the program either in Form I or Form II.

#### Coarse VOPT Procedure

Because of the normalized unity constraint, a variation of one step height for either coarse or fine tuning has an equal and opposite effect on the sum of the remaining voltage height variables. Therefore, the procedure for optimizing step heights is modified, as indicated in the following generalized procedure for optimizing the  $k^{th}$  step height. From this, (N-1) step heights are optimized by setting  $k = 1, 2, 3, \dots, (N-1)$ . The optimized value of the  $N^{th}$  step height is

$$VOPT(N,N-1) = 1 - \sum_{k=1}^{N-1} VOPT(k,k-1) \quad (10)$$

where VOPT(k,k-1) is the optimized value of the  $k^{th}$  step heights. For optimizing the  $k^{th}$  step height  $V_{m,m-1}$  for  $m = k$ , step heights that have been optimized thus far are kept constant at their respective optimum values, VOPT(m,m-1) for  $m = 1, 2, 3, \dots, (k-1)$ .

The initial values input to the program as VINIT(m,m-1) for  $m = 1, 2, 3, \dots, N$  are re-initialized, satisfying the normalized unity constraint. This is performed by finding the difference, called DIFF(m-1) for  $m=k$ , between the sum of the initial values of the first (k-1) step heights, and the sum of the optimized values of the (k-1) step heights

$$DIFF(k-1) = \sum_{m=1}^{k-1} VINIT(m,m-1) - \sum_{m=1}^{k-1} VOPT(m,m-1) \quad (11)$$

This difference DIFF(k-1) is equally distributed to the remaining (N-k+1) nonoptimized step heights as

$$VINIT(m,m-1) = VINIT(m,m-1) + DIFF(k-1)/(n-k+1) \quad (12)$$

for  $m=k, (k+1), \dots, N$ . The value of the optimizing variable  $V_{m,m-1}$  for  $m=k$  is renamed the current value VCURR. The optimizing variable is increased, in increments of VP, from the current value VCURR(1) to VCURR(J) in J steps within the window shown by Figure 11. Then, the corresponding change in value of  $V_{m,m-1}$  from its initial to the current value is calculated for each current value. This change, denoted by DELV(J) for the  $J^{th}$  step, is

$$DELV(J) = [VINIT(m,m-1) - VCURR(J)] \quad (13)$$

for  $m = k$ . The difference DELV(J) is distributed equally to the (N-k) steps by the equation

$$VINIT(m,m-1) = VINIT(m,m-1) + DELV(J)/(N-k) \quad (14)$$

for  $m = (k+1), (k+2), \dots, N$ . This re-initializes the (N-k) steps when the  $k^{th}$  step assumes the current value VCURR(J).

Using these step heights, and the optimum step width  $X_{OPT}$ , the program calculates the corresponding THD values. The value  $VCURR(L)$  of the  $k^{th}$  step height that gives the minimum value of THD in the coarse range  $THD(1)$  to  $THD(J)$  is the optimum value of the  $k^{th}$  step height  $VOPT(k,k-1)$ . Therefore,

$$VOPT(k,k-1) = VCURR(L) \quad (15)$$

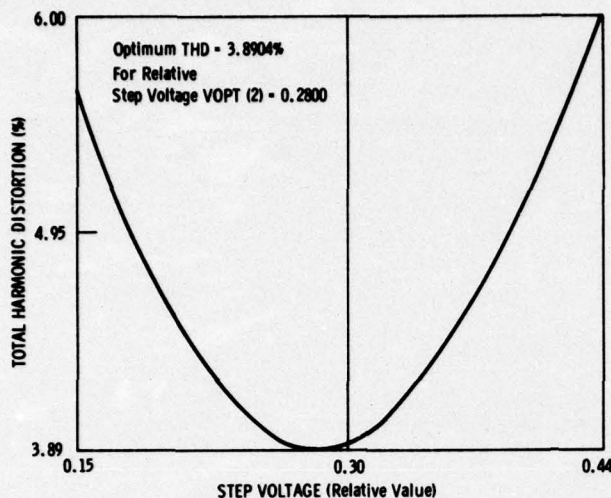


Figure 11. Effect of Step Voltage Variation on THD

#### Average/Fine VOPT Procedures

Average and fine optimization techniques like those used for step width  $X$  are applied and the optimum value is further refined. The optimization procedure is repeated (N-1) times until the (N-1) step heights are optimized, with the  $N^{th}$  step height obtained from equation (10). The program plots the THD values vs the optimization window for both coarse and fine tuning of each of the  $n$  variables. At this point, one iteration of optimization is completed, yielding optimized values of step width  $X$  and the  $n$  step heights.

For the next iteration, the optimized values become the initial values of the variables and the optimization procedure is repeated. This yields optimized values for the second iteration including the corresponding minimum THD (which is the optimum value in THD). Iterations are repeated a preset number of times, or are continued until a satisfactory degree of convergence is achieved. Using the "windowing" approach, and then proceeding to obtain an interim of optimization of each variable in turn, the overall convergence is well behaved, achieving levels of one part in  $10^{-3}$  routinely in 5 iterations or less.

If the number of step levels is sufficiently increased, the value of THD can be reduced to any arbitrary limit. In Figure 12, minimum (optimum) THD solutions are plotted as a function of the number of voltage taps on the inverter step autotransformer. The minimum THD points for this curve were computed with no constraints on the waveform design. The lowest possible THD varies from 16.6 percent

for one voltage tap to about two percent for nine voltage taps. The measurements of THD on inverter output waveforms closely agree with the calculated (optimized) values.

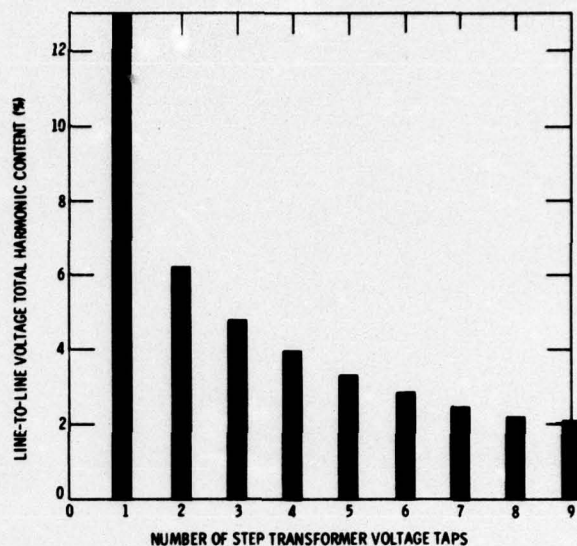


Figure 12. Affect on THD of Varying Voltage Taps, with Waveform Optimized Without Constraints

Results of a study of THD in waveforms designed under various constraints are summarized in Table 1. For the five conditions shown and with transformer voltage taps held constant (at three), values were computed of THD, magnitudes of the fifth and seventh harmonics, and conduction times of the power center thyristors. Each condition listed has an influence on inverter cost or complexity. The waveform designed under Condition 1, with no constraints, has the lowest THD and lowest values of 5th and 7th harmonics. This waveform would result in the smallest output filter, but also requires a relatively complex logic circuitry. The waveform designed to Condition 3 — with constraints of equal step widths, power center width a multiple of the step width, and zero dwell — has a wide power center and requires relatively simple logic circuits.

Shown in Figure 13 is an oscilloscope trace of an unfiltered inverter line-to-line output voltage waveform generated per Condition 3. Magnitudes of the significant nontriplen individual wave harmonics, before and after filtering, are listed in Table 2. Note that the measured THD of 5.6% corresponds to the computed value in Table 1, the highest for any condition.

The waveform designed per Condition 3 has equal, 10-degree wide step widths and a 110-degree wide power center. When step widths are equal, the highest-magnitude harmonics cluster around the step frequency harmonic. This is evidenced in Table 2, where the greatest harmonics — the 35th (2.88%) and the 37th (2.71%) — bracket the 36th harmonic, which is the step frequency. The release of harmonic energy around the step frequency simplifies the output filter.

CONDITION	DESIGN CONSTRAINTS	TOTAL HARMONIC DISTORTION (%)	HARMONIC MAGNITUDE (%) FIFTH	HARMONIC MAGNITUDE (%) SEVENTH	POWER CENTER WIDTH (Deg)	STEP FREQUENCY HARMONIC
1	None	4.78	0.10	0.21	100.2	
2	Equal Step Widths; Power Center Width = Multiple of Step Width; No Zero Dwell	5.25	0.48	0.73	100.0	27
3	Equal Step Widths; Power Center Width = Multiple of Step Width; Zero Dwell	5.6	0.98	1.46	110.0	36
4	Equal Step Widths	4.97	0.15	0.87	103.7	33
5	Equal Step Widths = $9^\circ$ ; Power Center Width Multiple of Step Width; Zero Dwell	5.43	1.78	2.4	117.0	40

\* Excluding Triplens

Table 1. Waveform Design, With and Without Constraints

HARMONIC NUMBER	MAGNITUDE (%)	
	BEFORE FILTERING	AFTER FILTERING
1	100	100
5	0.98	0.48
7	1.46	0.98
11	0.96	0.98
13	0.21	0.93
17	0.65	0.25
19	0.54	0.33
23	0.16	0.27
25	0.43	0.22
29	0.35	0.15
35	2.88	0.23
37	2.71	0.22
THD = 5.6%		2%

Table 2. Harmonic Breakdown

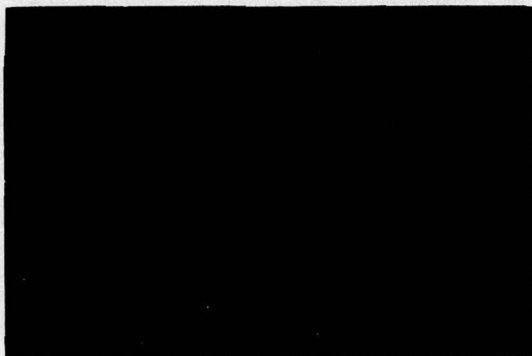


Figure 13. Unfiltered, Line-to-Line Voltage Waveform

#### SELECTION OF THD-DEPENDENT COMPONENTS

The quality of the inverter output voltage waveform (Figure 1), is determined primarily by the number of voltage taps on the step autotransformer. The lower the THD of the unfiltered waveform, the more thyristors are required in the inverter circuit. The higher the THD, the larger the output filter required to smooth the waveform to an allowable deviation factor. Inverters rated 10 and 15 kVA have been optimized, designed, fabricated and tested by Delco. Looking to the future, a study was made of these relationships to determine cost, volume, and weight for the THD-dependent components of a 100 kVA, 60 Hz inverter.

For this study, output filters were designed to produce inverter output voltages having two percent THD and deviation factor less than five percent when using from one to nine voltage taps. The number of thyristors used for the power center, phase selectors, and T+, T- are independent of waveform design. The required number of step thyristors<sup>5</sup> and the output filter capacitance vary with output voltage THD.

In calculating output filter capacitance, the total series inductance in the inverter was assumed constant for changes in the number of transformer taps. The following equations are used to compute total thyristor cost, and the filter capacitance required to produce a waveform with two percent THD.

$$\text{Thyristor Cost (dollars)} = (26 + 4n) \cdot P \quad (16)$$

$$\text{Capacitance (}\mu\text{F)} = K \frac{\text{THD}}{n} \quad (17)$$

where  $n$  = Number of step transformer voltage taps  
 $P$  = Thyristor cost in dollars  
 THD = Total harmonic distortion of the unfiltered inverter output voltage  
 $K$  = Constant ( $\mu\text{F}/\%$ )

Figure 14 shows the variation in cost of the inverter thyristor assembly, plus output filter capacitors with increased use of taps.

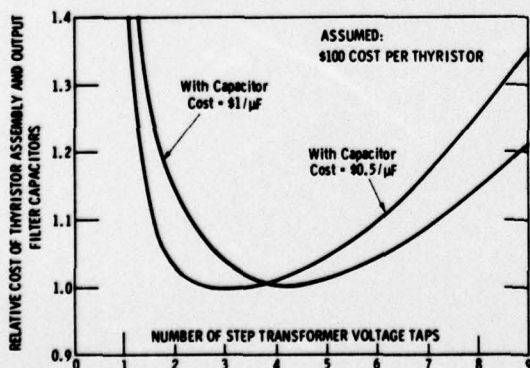


Figure 14. Affect on Component Cost of Varying Voltage Taps

Assuming a cost of \$100 per thyristor and \$.50 per microfarad, a minimum-cost 100 kVA inverter would have three step transformer voltage taps. If the capacitor cost were \$1 per microfarad, the minimum cost system would have four taps. The 4-tap transformer selection would also provide minimum weight and volume of these components, as illustrated in Figure 15. Selection of three voltage steps, however, would involve only a 5% penalty in size and weight.

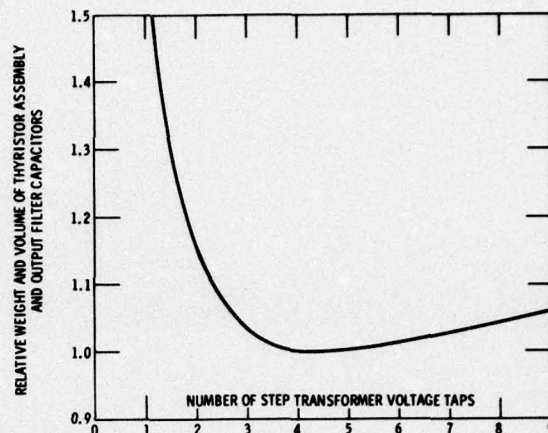


Figure 15. Affect on Component Size of Varying Voltage Taps

#### SUMMARY

The Delco inverter configuration allows tradeoffs between waveform design and inverter cost without major changes in the circuit design. When no constraints are imposed in the waveform optimization, selection of the number of voltage taps ( $n$ ) on the step autotransformer defines the minimum THD obtainable in the unfiltered output voltage. Selection of  $n$  also determines the total number of circuit thyristors and the approximate size of the output filter.

When a constraint is introduced in waveform design, such as equal step widths, it impacts the cost of the inverter. The effect of the constraint is to shift the distribution of harmonics such that they peak at the step frequency. In terms of circuit design, this allows use of less complex logic circuitry and a simpler output filter design, while incurring slightly greater THD. An increase in power center widths will improve inverter efficiency, but also increase THD.

The step autotransformer and associated switching circuits simultaneously generate Y and X step voltage functions at a frequency three times the inverter output frequency. The commutation circuit used to turn off the step selector thyristors connected to the double bus has a constant energy source independent of inverter input voltage or load.

The application of a U.S. Army MERDC computer program by Delco for waveform optimization exemplifies how, in pursuit of a design goal, the development costs are minimized through joint use of Government and contractor facilities and capabilities. In this instance, considerable hardware fabrication and testing were avoided by the availability and flexibility of the computer analysis capability.

The circuit improvements discussed herein demonstrate the design maturity of the Delco step wave power center inverter, developed for a family of military solid state power conditioners, and applicable to any commercial/industrial use requiring high reliability, high quality output power. While operating experience and test data have primarily been acquired on operating hardware in the 10 to 30 kVA range, inverters rated up to 100 kVA can be fabricated with present technology and materials with very low development risk.

<sup>5</sup> U.S. Patent No. 3,859,584